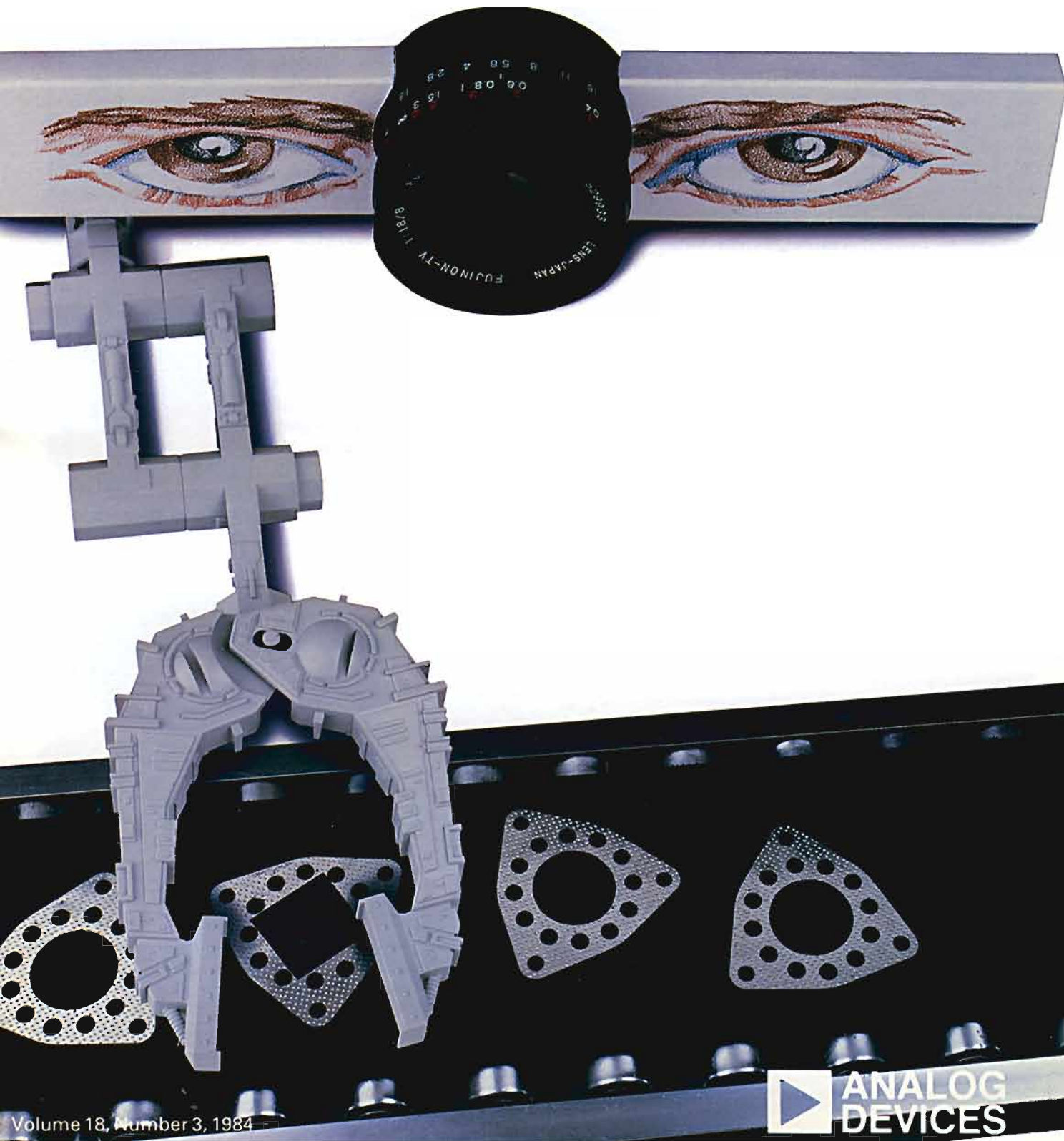
analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing



Volume 18, Number 3, 1984

ANALOG DEVICES

Editor's Notes

COVER THEMES

Our cover themes are symbolic but usually self-evident. Certainly, the present cover—showing an aberrant gasket being identified by The Eye™ and about to be whisked away by a robot arm—leaves little to the imagination.

However, we have had a few questions about the last issue's cover; a typical comment was, "It's beautiful, but what is it?" The artist's answer: It is supposed to symbolize *evolution* of 12-bit monolithic DACs, from the switch-and-ladder-only AD562 to the complete double-buffered AD667, with its on-chip amplifier and reference. The tool in the foreground has liberated the AD667, the top stratum, from its ice-age prison. In the background are still-embedded predecessors, including—dimly seen—dinosaurs.

BARRIE GILBERT: IEEE FELLOW

We are pleased to note that Barrie Gilbert has been named a Fellow of the Institute of Electrical and Electronics Engineers (IEEE) "For the discovery of the translinear principle and invention of the translinear multiplier." According to the IEEE's bylaws, the status is "conferred only by invitation of the Board of Directors upon a person of outstanding and extraordinary qualifications and experience in [the IEEE-designated fields], who has made important individual contributions to one or more of these fields."

Barrie, a Division Fellow at Analog Devices (one of the highest levels of technical advancement within the Company),[1] manages the Semiconductor Division's Northwest Labs, in Forest Grove, Oregon. He authored the article, beginning on page 12 of this issue, describing the AD639 monolithic analog trigonometric function generator—one of the many Analog Devices products he has either designed or been fundamentally responsible for. He has also made numerous contributions in circuit design, product proposals, application ideas, and process technology.

A prolific designer and writer, with a wide range of interests, Barrie has sixteen patents, more than 50 publications, five "Outstanding Paper" awards from the International Solid-State Circuits Conference, and the IEEE 1970 Achievement Award (for a paper that led to the subsequent development of integrated injection logic—I^2L).

Barrie was born in Bournemouth, England. His vocation in electronics first surfaced when he built an oscilloscope at age 12. He subsequently received the HNC (Higher National Certificate) in Applied Physics (with honours) from Bournemouth Municipal College in 1962, and has taught circuit design at universities in Europe and the United States. Before joining Analog Devices, he worked at Mullard, Tektronix, and Plessey. ▶

Dan Sheingold

[1]See "Analog Devices Names Division Fellows," *Analog Dialogue* 14-1 (1980), page 15.

THE AUTHORS

Alan Berger (page 3) joined ADI's Machine Vision Products Group (MVP) early this year as a Senior Marketing Specalist. He received a BA degree from the University of Michigan and an MS from MIT's Sloan School of Management. Alan brings to his job at ADI several years of experience in the machine-vision industry.

Geoffrey Boyes (page 16) is divisional Promotions Manager at ADI's Memory Devices Division, in East Molesey (Surrey), England. Graduated in 1968 from London University, he received a B.Sc. degree (honours) in Physics. He worked as an Engineer in radar data processing at Marconi Radar, then as an instrument sales engineer. At ADI, he has had several positions in Sales and Marketing management. His interests include music and renovating old houses.

James Bryant (page 19) is European Applications Manager for ADI, based in Newbury, England. A graduate of the University of Leeds, he earned a B. Sc. in Physics and Philosophy. He has 15 years of applications experience, at both Plessey and ADI. James has numerous publications on a wide range of topics and served as a technical advisor to Parliament on CB radio. His diverse interests include amateur radio (G4CLF), collecting science fiction (> 3,000 volumes), hypnotism, and parapsychology.

John Croteau (page 15) is a Product Marketing Engineer in the Converter Group at Analog Devices Semiconductor. He has a B.S.E.Sc. from Penn State and is pursuing an M.B.A. part-time at Boston University. His undergraduate honors project and thesis involved research, design, and processing of solar cells and optoelectronic devices. Since joining ADI, his projects have involved the interfacing of a/d and d/a converters to μPs and μCs.

(continued on page 26)

analog dialogue

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IVS-100

THE EYE™ – An Intelligent Vision System for Industrial Image Analysis

by Alan Berger

The IVS-100 is a powerful machine-vision development system recently unveiled by the Machine Vision Products group of Analog Devices. Dubbed THE EYE™ from Analog, the IVS-100 combines extensive processing capabilities with proprietary machine-vision software to provide a complete development package for industrial image analysis. This article introduces machine-vision concepts and the IVS-100 system.

WHAT IS MACHINE VISION?

Machine vision, also called intelligent vision or computer vision, is analogous to the human eye/brain system. A device for image acquisition, such as a video camera, serves as the eye; and a computer serves as the brain. Analog signals from the camera are digitized, and the digital information is processed and analyzed by the computer. Based on the results of the analysis, the computer makes decisions about the object or scene being viewed. This three-step process—image formation, image analysis, and image interpretation—is basic to any machine-vision system.

During image formation, light from an object or scene enters the video camera and is converted to a series of analog electrical signals. Before they can be used by the computer, these signals must be sampled, digitized, and organized into an array of image data. This process can be thought of as breaking down a continuous image into thousands of discrete picture elements, or *pixels*. The *spatial resolution* of an imaging system refers to the number of pixels into which the original image is digitized. Most vision systems currently available can resolve images into arrays having spatial-resolutions ranging from 128 × 128 (= 16,384 pixels per image) to 512 × 512 (= 262,144 pixels per image).

In addition to spatial resolution, there is another image attribute

fixed during the image-formation stage, *intensity resolution*. The continuous range of light intensity existing in the original analog signal produced by the video camera is divided into a number of gray levels (i.e., *quantized*) during conversion from analog to digital. Each pixel is associated with a gray level corresponding to the light intensity observed at its position in the image.

In the case of a binary imaging system, employing a single bit of intensity information, the "gray scale" consists of only two values—full white or complete black. The more bits used to encode the pixel light intensity, the better the gray-scale resolution—and the greater the retention of information that was present in the original image. The highest-fidelity systems on the market digitize the intensity information to eight bits, corresponding to 256 discrete levels of gray.

Prior to image analysis, some vision systems, using dedicated hard-

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ware in the image-acquisition module, preprocess the digital image to minimize noise and to enhance contrast.

Since feature information is necessary to interpret an image, the goal of image analysis is to extract image features and to describe or measure them. A large variety of feature-extraction algorithms are available for processing either the image as a whole or individual regions within the image. The geometry, position, and gray level of regions having homogeneous intensity are among the features of potential interest. Figure 1 shows how gray-scale resolution can affect feature extraction.

Finally, the vision system must interpret the image based on its observed features. The system's task is to compare what it has learned about the object or scene that is being inspected with information stored in memory regarding other images of a like type. For example, if the analysis reveals a two-inch square shape with a one-inch-diameter hole in the center, and this matches—within specified tolerance levels—a model of the same kind of part stored in the system memory, the interpretation made by the system might be, "Yes, this is a good part." The system might then go on to signal production equipment to sort the part to a particular "good" bin.

WHERE CAN MACHINE VISION BE USED?

Machine vision can be considered for many industrial applications for which human vision is now being utilized. A comparison of human vision capabilities with those of machine-vision systems helps to identify those applications that are the most attractive candidates for machine vision solutions:

- Machine-vision systems are capable of operating at speeds an order-of-magnitude faster than human vision.
- Machine-vision systems can perform exacting, repetitive tasks without a break; human operators are subject to distraction, fatigue and boredom, factors which can quickly lead to performance degradation. Moreover, it has been shown that, as the quality of inspected parts improves, human inspection performance actually declines—it's far easier to find one bad part in ten than one in a thousand.
- Machine-vision systems are able to make consistently precise quantitative measurements; most people, on the other hand, are capable of making only rough size estimates.
- Machine-vision systems can interface directly, and at compatible data rates, with other types of production equipment; the human interface with production equipment is comparatively slow and prone to error.
- People are clearly superior to machines in situations requiring the exercise of judgement, e.g., when novel problems arise; currently available machine-vision systems can handle only a relatively small range of possibilities.

From this comparison, we infer that the kinds of inspection tasks that are prime targets for machine-vision solutions are highly repetitive and require speed, precise measurements, or identification of defects—and interfacing with production equipment. The resulting large number of potential applications can be generally divided into three major categories: inspection, measurement, and robot guidance.

The requirement for visual *inspection* of products cuts across a broad spectrum of industry. Inspection data are used both for making go/no-go decisions regarding product quality and for logging information on an item-by-item basis to trace production history. Industries with critical requirements for visual inspection include electronics, auto and aerospace, and packaging.

Assessing the dimensional *accuracy* of parts, sub-assemblies, and the finished product is a potential application for machine vision in a number of industries. Although—given unlimited time for measurement—present vision systems can not achieve as high a degree of accuracy as other measurement systems (such as optical comparators), they have the advantage of being able to perform 100% inspection of products that are moving at high line speeds.

In the area of *robot guidance*, machine vision can be used in several ways: in finding and sorting parts; in directing activities such as welding, spray-painting, deburring, etc.; and in assembly operations. At present, the auto industry is by far the largest user of machine-vision systems in conjunction with robots.

In summary, inspection, measurement, and robot guidance account for the bulk of current machine-vision applications; inspection and measurement each contribute roughly 40% of the total. The present (1984) market size, estimated to be $70 million, is conservatively expected to grow to more than $500 million by 1990, reflecting a 40% cumulative average growth rate.

WHAT IS THE IVS-100?

The IVS-100 is a state-of-the-art intelligent vision system for image acquisition and analysis. It is a development system designed to meet the challenges of today's industrial automation problems in inspection, measurement, and robot guidance. The basic system hardware includes:

- Image Acquisition and Display Module (Frame Grabber)
- Central Processing Unit (CPU Board)
- Winchester and Floppy Disk Storage
- Video Camera
- Video Monitor
- Display Terminal

Figure 2 shows the physical interrelationship of these basic building blocks in the IVS-100 system. They are divided into three groups: 1) the IVS-100 master unit; 2) image acquisition and display peripherals; and 3) user interface peripherals. The IVS-100 master unit contains the disk drives in addition to the CPU and frame grabber boards indicated in the diagram. The display terminal, camera (including power supply), and video monitor are furnished with the standard IVS-100 system, while the peripheral items indicated by dashed lines (e.g., parallel port devices, external trigger source) are supplied by the user.

The *frame grabber* is the image-acquisition front end for the computational hardware. It is responsible for digitizing the camera image and assigning gray-scale values to the resulting pixels. Major design features of the IVS-100 frame grabber include the flexibility of variable spatial-resolution modes (up to a maximum of 512 × 512), high-intensity resolution (256 levels of gray scale), two image memories (or buffers), and image-preprocessing hardware.

The *CPU board* also supports a number of advanced features useful for real-time machine-vision applications. Processing power is provided by state-of-the-art Intel* microprocessors: an 80286 main processor, an 80287 numeric coprocessor, and an 80186 input/output (I/O) coprocessor. Because the numeric and I/O coprocessors are incorporated into the CPU design, the 80286 main processor is relieved from a variety of time-consuming chores; the result is enhanced system throughput. The CPU is provided with one megabyte of main memory, readily expandable to two megabytes via a piggyback memory option.

Software for the IVS-100 can be divided into three major areas: 1) the Concurrent CP/M* (CCP/M) operating system, 2) programming languages, and 3) machine-vision software. CCP/M is a real-time, multitasking operating system well suited to machine-vision applications. The CCP/M package from Digital Research includes the operating system proper plus a variety of utilities useful for program development.

Programming languages available for the IVS-100 include three high-level languages—C, FORTRAN-77, Pascal—and a relocatable assembler. All four languages come from Digital Research, and all produce compatible object code. Thus, code modules written in any of the languages can be incorporated into a single application program.

The operating system and language capabilities of the IVS-100 provide a powerful and flexible environment in which machine-vision applications can be implemented. However, the *machine-vision software* produced by Analog Devices forms the heart of such applications. This software, included in the IVS-100 Library provided with the standard system, contains a large number (more than one hundred) of machine-vision primitives and related routines which take full advantage of the IVS-100's advanced capabilities. ▶

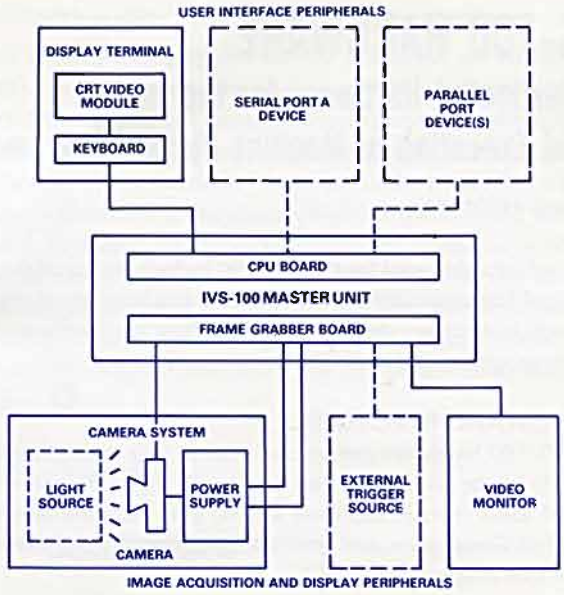


Figure 2. Block diagram showing interrelationship of major IVS-100 components. User-supplied components are indicated by dashed lines.

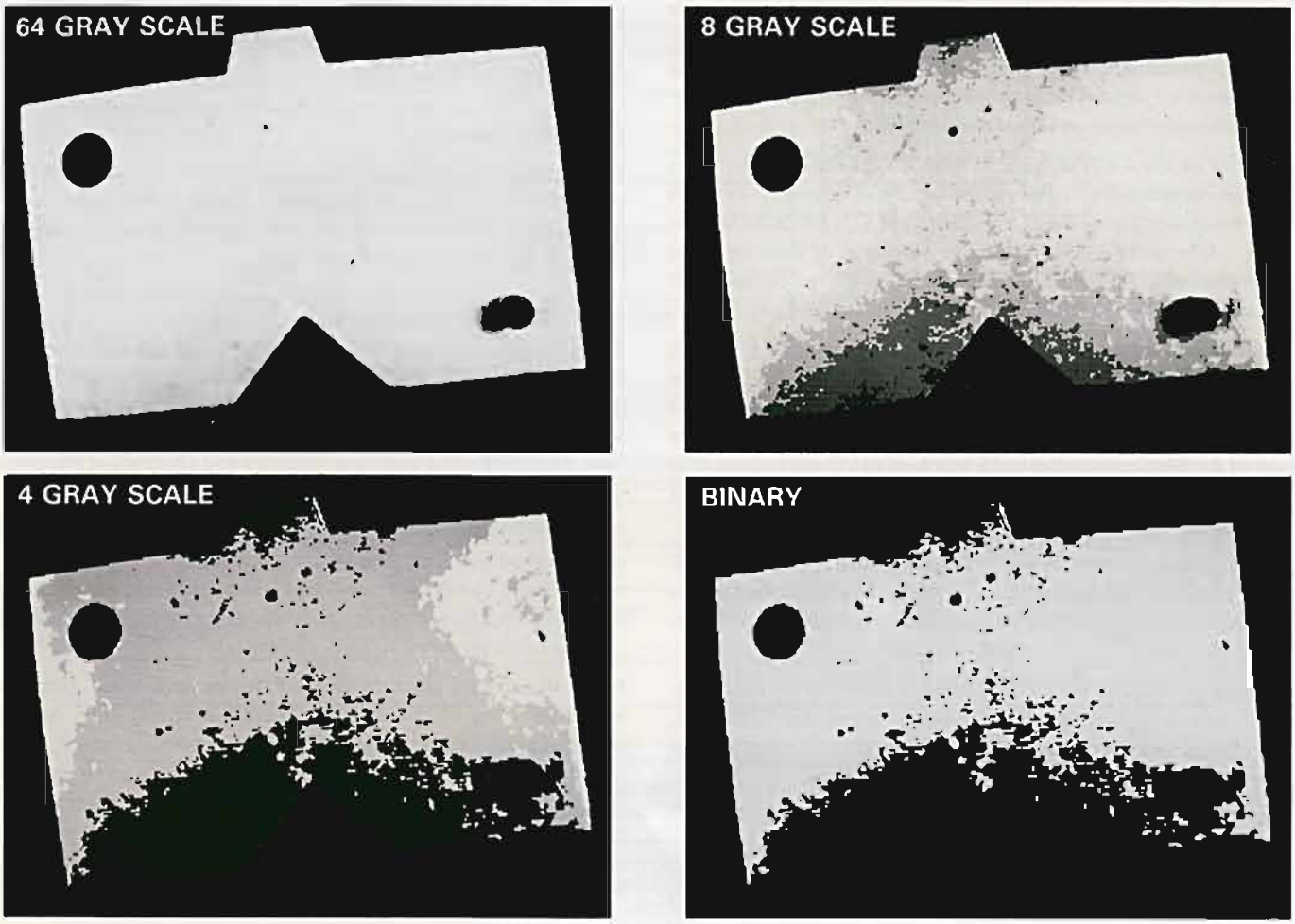


Figure 1. This series of photographs show clearly the advantages of high intensity resolution. With 64 levels of gray, part boundaries are distinguishable from background; and fine features, such as the shadow cast by the post in the lower right-hand corner, are discernible. Using fewer levels of gray renders the scene more subject to the effects of shading (note the deterioration of the lower, slightly shaded portion of the part), and obliterates subtle features.

*Intel is a registered trademark of Intel Corporation. Concurrent CP/M is a trademark of Digital Research Inc.

IVS-100 HARDWARE

Sophisticated Hardware for the Rapid Execution of Machine-Vision Programs

by Reg Gillmor

The hardware designed for the IVS-100 includes many of the most advanced features currently available for machine-vision systems. This article describes these features and how the hardware functions in an application environment.

SYSTEM ARCHITECTURE

The IVS-100 hardware can be classified in four major functional areas: 1) image acquisition and display; 2) the central processing unit; 3) mass storage facilities; and 4) user interface hardware. These functional units, and their various sub-units, are illustrated in the block diagram of Figure 1.

In the IVS-100 system diagram of Figure 1, the topmost block denotes the IMAGE ACQUISITION AND DISPLAY module. Besides the video camera and video monitor, it includes a printed circuit (PC) board in the IVS-100 master unit, known as the "frame grabber." The frame grabber's function is to acquire the image in digital form, to store the image in frame memory, and—when desired—to perform certain preprocessing operations involving newly acquired data. For multiple-camera installations, an optional camera multiplexer board is available.

The heart of the CENTRAL PROCESSING UNIT (CPU) is an 80286 microprocessor, supported by an 80287 numeric or math coprocessor, occupying the block labelled MAIN PROCESSOR in Figure 1. The 80287 is for the rapid execution of floating-point (i.e., real-number) operations. These state-of-the-art components are members of the Intel* 8086 family of 16-bit processors.

An additional state-of-the-art Intel microprocessor, the 80186, labeled I/O PROCESSOR, has been incorporated in the CPU design to control input and output functions. In performing the I/O processing, the 80186 unburdens the 80286 main processor from many of the time-consuming tasks involved in I/O operations. The multiple-processor structure, offloading both math and I/O, is a key to the excellent speed performance of the overall system.

The three processors are located in the master unit on a single PC board. This CPU BOARD also contains the hardware needed for the various I/O interfaces (serial I/O, parallel I/O, and disk I/O) indicated in Figure 1.

Other components on the CPU board (not shown in the block diagram) include programmable read-only memories (PROMs), which contain start-up, diagnostic, and similar local programs for the 80286 and 80186 processors; 16 KB (kilobytes) of RAM (random access memory) for use by the 80186 during I/O operations; and various processor support chips.

The CPU's main memory is also located on the CPU board. It consists of 1 MB (megabyte) of RAM. An additional megabyte of memory can be made available through a piggyback memory option.

Another CPU option shown (dashed lines) in Figure 1 is the IMAGE ARRAY PROCESSOR, a self-contained single-board discrete-component processor. It can be thought of as an auxiliary CPU to speed up execution of most of the routines included in the IVS-100 Library of image-processing software. Because it enhances overall system speed, it is also called the *accelerator board*. As indicated in the block diagram, the accelerator board has a private bus for direct access to the frame memory (RAMs) on the frame grabber board.

MASS STORAGE for system software, application programs, and image data is provided by a 15 MB Winchester disk and a 5 1/4" floppy-disk drive. The floppies are double-sided and double-density formatted, with a resulting storage capacity of 640 KB apiece. Optionally, the two disk drives (hard and floppy) can be eliminated from the master unit and replaced by a non-volatile memory board.

The USER INTERFACE consists of an operator interface and an application interface. The primary interface between an operator and the IVS-100 is a display terminal. It can be supplemented by an optional joystick or printer on the second of the IVS-100's two serial I/O ports. The second port can alternatively be configured to connect with a host computer—or other devices requiring high-speed communication.

The application interface consists of user-specified automation devices or other production equipment. These can be connected to the system via the serial or parallel I/O ports. The arrangement depends on the specifics of the application.

SYSTEM OPERATION

When starting up, the system performs a variety of diagnostic tests to ensure that all components are functioning properly. The operating system is then loaded from disk into main memory. If an application program has been developed and is available on disk, it can be loaded into main memory and executed at this point.

This is the sequence of operations in a typical application: the IVS-100 acquires an image of the object to be inspected; it extracts feature information from the image for comparison with a stored model of the object's features; and it then sends the results of this comparison to mass storage for data logging, to an external device capable of taking some action—or both.

Image acquisition begins with the video camera, which generates sequential rows of analog pixel (picture-element) data. A single frame of pixel data, corresponding to one complete image, will be transferred serially to the frame grabber hardware on receipt of an internally or externally generated trigger. Internal triggers are generated by the application software. Depending on the application, external triggers are generated by such devices as photo cells, microswitches, production equipment, host computers, programmable controllers, or the display-terminal's keyboard.

Once the system is triggered, the video signal is sampled and passed through an 8-bit analog-to-digital converter (A/D in Figure 1), which digitizes the pixel light-intensity information into 256-level gray-scale data. The array of digital pixel data corresponding to the original video image can then be stored in the image buffers (512 × 512 × 8-bit RAMs) on the frame-grabber board; there the

*Intel is a registered trademark of Intel Corporation.

data will be accessible to the CPU (and optional image array processor). The image buffers are also accessible to the on-board digital-to-analog converter (D/A), which restores the intensity information to analog form for viewing on the video monitor.

Besides making the raw image data available to the rest of the IVS-100 system, the frame-grabber board can perform a degree of image preprocessing, in order to reduce follow-on processing time. The preprocessing hardware (PREPROCESSOR in the block diagram) includes an arithmetic logic unit (ALU) and a look-up table (LUT). The ALU, in conjunction with paired image memories, can perform such preprocessing routines as summation and averaging of multiple images. The LUT can be programmed to perform point transformations of individual pixel values as part of preprocessing routines, such as thresholding and contrast enhancement.

Further image processing and feature extraction are handled by the CPU and—if present—the accelerator board (image array processor). The execution of image-processing and feature-extraction routines prepares the way for image interpretation, i.e., the actual identification or verification of the object under inspection. The set of features identified in the observed object is compared with the expected, or model, feature-set to calculate goodness-of-fit and similar measures of correspondence. The results of this analysis can be logged into one of the mass storage devices or used to generate application-specific control signals, which are communicated to the external hardware via the serial or parallel I/O interfaces. ■

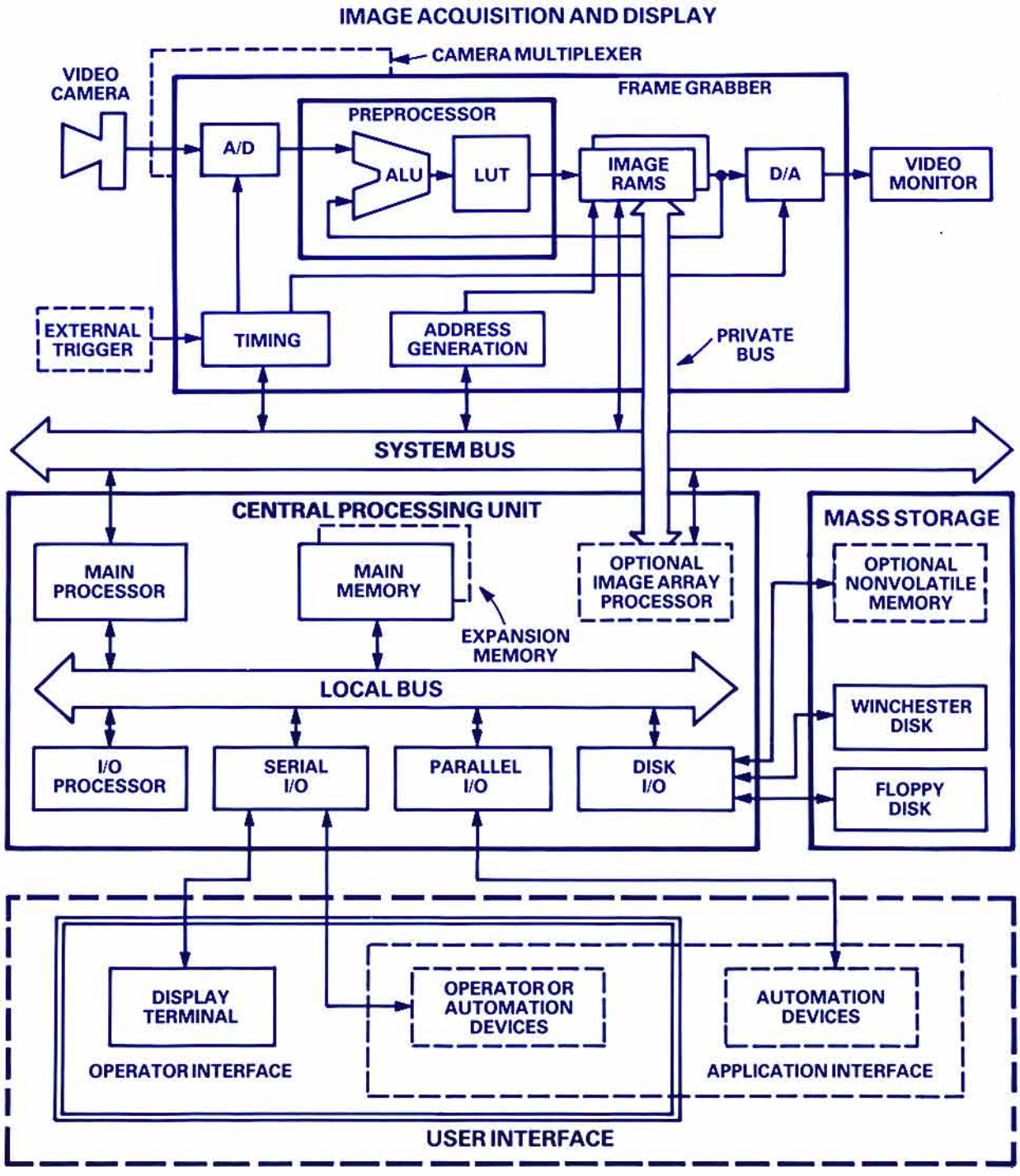


Figure 1. IVS-100 simplified block diagram. Optional components are indicated by dashed lines.

IVS-100 SOFTWARE

A Comprehensive Machine-Vision Library Facilitates Applications Programming

by Patrick Helsingius and Steve Zoeller

Efficient algorithms, specifically designed for use in machine vision, are the key to powerful and versatile machine-vision programs. A major feature of the IVS-100 development system is its library of machine-vision routines, which make effective use of all the system hardware's capabilities. The availability of these routines, which distinguish the standard Analog Devices system package from many of its competitors, is regarded as a significant advantage of our system. This article presents an overview of the IVS-100 Library and some examples of how the library's routines can be used for industrial image analysis.

LIBRARY OVERVIEW

Because machine vision is used both to gather information in a scene and to analyze it, a variety of image-processing and analytical routines are required. In addition, routines are needed which relate directly to the system hardware so that, if advanced hardware capabilities are present, they can be utilized effectively and efficiently. The IVS-100 library comprises both kinds of routines.

Library routines are organized into the following six categories:

- Region and Boundary Routines
- Math Routines
- Single/Double Integer Routines
- Joystick/Mouse Routines
- Frame-Grabber Routines
- Mass Storage and Memory Manipulation Routines

Region and boundary routines provide for the identification and manipulation of regions and boundaries within images. Examples include the locating of homogeneous regions (also known as "blobs"); the determination of boundaries (edges) by gradient techniques; and the partitioning or merging of blobs.

Math routines are used for both statistical and deterministic analyses of image regions, boundaries, and other parameters. Examples of these include curve-fitting routines, various matrix operations, and routines for generating histograms.

Single/double-integer routines allow basic arithmetic operations to be performed on signed, 32-bit, fixed-point quantities, as well as for conversion between 32-bit and standard 16-bit quantities. Virtually all mathematical manipulations in machine vision are accomplished using 16- and 32-bit signed, fixed-point numbers.

Joystick/mouse routines are included for the control of these optional devices. They are useful during the training of the system on a new part or scene to be inspected.

Frame-grabber routines perform pre-processing operations involving the frame-grabber image buffers, and they set various parameters for other frame-grabber hardware. Examples include routines for summing images using the frame-grabber ALU and for transforming pixel values (i.e., gray-scale levels) via the look-up table.

Mass-storage and memory-manipulation routines control memory configuration, memory access, and general disk I/O.

LIBRARY USAGE

The central task of an industrial vision system is to extract information from an image and arrive at decisions based on this information. In the first phase of image analysis, the raw pixel data may require processing to produce an image more readily usable during follow-on analysis. This sort of *preprocessing* often involves the exploitation of the frame grabber's processing capabilities.

Image preprocessing results in the transformation of individual pixel gray-scale values in such a way that features present in the original image but hard to see become more distinct, both to the human eye and to the machine-vision system. Preprocessing can also be used to simplify the image (compress data) so that subsequent processing is more efficient. Histogram creation illustrates both of these potential uses of preprocessing.

An intensity histogram of an image—or portion of an image—counts and indicates the number of pixels occurring at each possible gray level (Figure 1). For example, if the image is generally dark, most of the pixels will be bunched at the lower gray-scale levels, with few (if any) occurring at the brighter end of the intensity spectrum. Once the intensity histogram of an image is calculated, other routines can be implemented, using the preprocessing hardware to modify the distribution of gray levels in the image.

If, for example, the image is dark (as above), it might be helpful to increase contrast. This can be done by flattening the image histogram and "stretching" it across the available range of gray scale, a technique referred to as histogram equalization. A flat—or equalized—histogram corresponds to a uniform distribution of

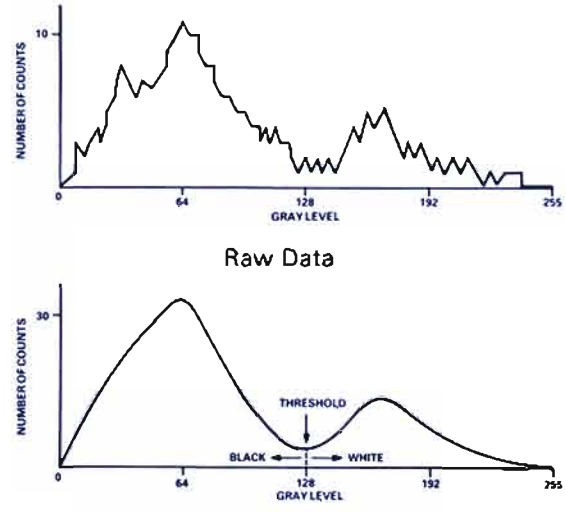


Figure 1. Histogramming routines available in the IVS-100 library can be used to smooth the histogram function and then automatically set a threshold value for generating binary (black-and-white) images from a gray-scale image. This example illustrates the smoothing of a bimodal histogram and the setting of a threshold value between the two peaks of the smoothed curve.

gray levels within the image. This increases contrast, improving the detectability of many image features.

Another use of intensity histograms is in setting thresholds for binary (black-and-white) images. It is not always necessary to have a wide range of gray-scale data available to represent the feature(s) of interest adequately in an image to be processed. Sometimes a simple black-and-white image will do. When feasible, a binary image is preferable to a gray-scale one because it can be processed in a much shorter time.

By analyzing the intensity histogram in the original image, one can determine the best threshold value for generating a binary image. Pixel values below this threshold will be set to black, while those at or above the threshold will be set to white.

Once the quality of the image has been improved—or the data simplified—via preprocessing, analytical routines can be applied to segment the image and extract features of interest. The key step in this process is the determination of boundaries. Much of the information found in an image is contained in region boundaries. If they exist, boundaries are locally continuous. However, owing to poor image quality or other factors, the boundary of an object or region might appear to be locally discontinuous. This potential difficulty can be overcome by first locating local edges in the image and then composing edges together into boundaries.

Edges, which by definition correspond to intensity discontinuities in the image, can be located using various edge detectors or operators included in the IVS-100 Library. In contrast to the point operations involved in the histogram-modification techniques mentioned above, edge detectors rely on neighborhood operations; i.e., the intensity value of a pixel is modified on the basis of its neighbors' values, not just its own.

Among the many edge detectors available, Sobel's gradient operator is one of the better known. As with many other neighborhood operators, its use entails the convolving of the image against a 3 × 3 mask or kernel. That is, a weighted mean is computed for each pixel in turn as a 3 × 3 mask of weights for the pixel of interest (in the center of the mask) and its eight nearest neighbors is "slid" across the image. Different edge operators assign different sets of weights. Sobel's gradient operator uses the following kernels:

A.
$$\begin{matrix} -1 & 0 & 1 \\ -2 & 0 & 2 \\ -1 & 0 & 1 \end{matrix}$$

B.
$$\begin{matrix} 1 & 2 & 1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{matrix}$$

There are two kernels, at right angles, because edges are detected in two dimensions, vertical and horizontal. The vertical detector (A) will be most sensitive to perfectly vertical edges in the image. Suppose that we have such an edge and that the vertical mask is centered on it. The three pixel values on the left might be high corresponding to a light background, and the three on the right low corresponding to a dark object. Applying the indicated weights to calculate a mean value for the center pixel will, in this case, result in a relatively large negative number. If the background were dark and the object light, a large positive number would result. In other words, large values, whether positive or negative, correspond to large gradients in the intensity data.

If, on the other hand, the kernel were applied in an area of the image showing little or no changes in intensity, i.e., where there is no edge, the Sobel operator generates a low absolute value. Applying both the vertical and horizontal kernels to the image and combining their results leads to an output image in which local edges are bright and other areas dark.

Although there are various ways to determine boundaries from a given set of local edges, using a priori information is perhaps the best. That is, if you're inspecting a known part, you already know what sort of boundaries to expect. In industrial image analysis, this is almost always the case, and using this knowledge is at the heart of the *model-based approach* to part identification, an approach taken by Analog Devices for some IVS-100 applications.

In the model-based approach, a model of the part to be inspected is created in memory by first acquiring an image of a perfect ("golden") part. This image is then processed and analyzed to determine the length, curve types, and intensity gradients of object boundaries, both external (perimeter) and internal (surface features). A model of the part is developed, based on the extracted features and the mutual relationships of these features; thus, the model is a *syntactic* one.

With a model of the expected image in memory, the vision system can conduct a hierarchical search within a sample image for the part under inspection (Figure 2). The search begins by looking for an edge transition with a specified gradient. By concentrating first on the gradient information, a large amount of extraneous information in the image can be ignored. When the expected edge transition is found, the system will go on to look only in areas of the image where the model suggests it can find features which will uniquely determine the orientation of the part in the field of view. This continues until such a unique orientation is obtained. With the part identified and its orientation determined, various measurement or part-manipulation procedures are now possible. This model-based approach is applicable to a wide variety of machine-vision problems ▶

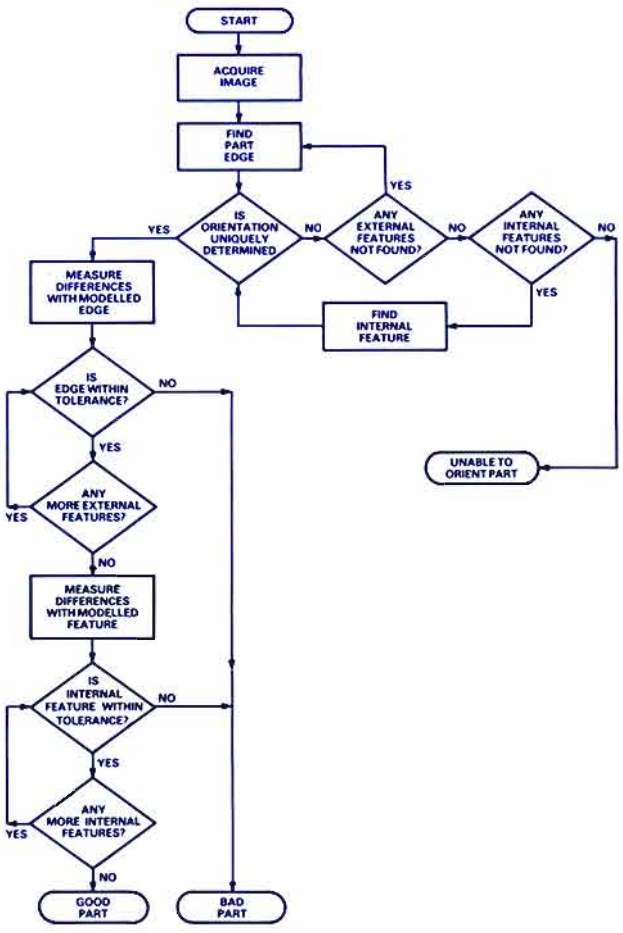


Figure 2. Sample flow chart for a parts-inspection program using the model-based approach.

IVS-100 APPLICATIONS

Opportunities for Machine Vision in the Electronics Industry Are Especially Plentiful and Promising

by Sandra Perry and Kimberly Mager

Worldwide, the automated manufacturing process is undergoing major modifications. The factory is evolving from a fixed automation environment toward a more flexible environment in which production equipment is, to an increasing degree, able to monitor, modify and guide itself through the production process. Machine vision can make substantial contributions to flexible manufacturing environments, and nowhere is this versatility more apparent than in the electronics industry. This article presents a survey—by no means complete—of machine-vision applications in electronics.

INTEGRATED-CIRCUIT FABRICATION

Integrated circuits (ICs) begin as wafers of silicon. Machine vision can be used to inspect the raw wafers for defects and to track the wafers as they travel through the IC fabrication process. Wafers can be tracked by character-reading vision systems which view and record numbers laser-etched onto the wafers. The information gained by machine inspection is used to improve process control.

During probe testing of chips on a wafer, a code indicating test results can be laser-etched on each chip. After the wafer is scribed and separated into dice, a vision system may be used to read the code on each die, sort the good from the bad, and keep track of the overall rates and types of defects.

During the IC assembly process, die mount, wire bond and pre-cap or "third-optical" inspection are additional opportunities for automated inspection. *Die mount* is already automated in many factories. The orientation of the die is critical to proper performance of the device, but most automatic mounting machinery does not yet have feedback capability to correct for misalignment during the mounting process. A vision system that checks the orientation of each die as it is placed in the package prevents mounting errors.

Automated *wire bonders* already use vision systems for an elementary form of pattern recognition. These devices locate registration marks on a die and its package and then proceed with the automated wire-bonding process. There is no provision for making corrections during bonding; once the registration marks are located, the system runs blind until it encounters the next package. A more advanced vision system would allow the bonder to find each pad and correct for any local variations.

Third-optical inspection, which occurs just prior to device sealing, is another area ripe for automation. The automation already in place during the earlier stages of IC fabrication is resulting in an expanded need for faster and more accurate inspection methods to keep up with the flow of assembled ICs ready for sealing. High-performance devices require 100% inspection; without automation, this step in the manufacturing process is a major bottleneck.

Third-optical inspection is not easy. It requires the vision system to look for chips, cracks, and scratches in the die or substrate, and for proper mounting of the die in its package. The system must also insure that wire bonds are present, complete, and on the pad to a specified tolerance. To perform these tasks effectively, full gray-scale processing will be necessary, and performance speed will be critical.

HYBRID ASSEMBLY

Uses of machine vision during hybrid assembly are similar to those outlined above for ICs, but because hybrids involve several dice mounted within a single package, the technical problems are more complex. Moreover, hybrids are more often made in small batches rather than in the long runs common with many monolithic products. Consequently, the vision systems used for hybrids must be flexible, easily switched from inspecting one type of part to another.

A category unique to hybrids is the inspection of thick-film substrates. Using machine vision to inspect each layer of a thick-film substrate for shorts, opens, and trace dimensions would improve yields greatly by removing defective materials from the manufacturing process before additional time and materials are spent. Again, the inspection problem is a difficult one; line widths and spacing are constantly decreasing, leading to greater and greater numbers of connections to inspect per-unit-area. In this respect, hybrid substrates are similar to another product in the electronics industry requiring inspection—bare printed circuit boards.

PRINTED CIRCUIT BOARDS

Electrical inspection of bare PCBs can only be done after the fabrication process is complete. Inspection of the inner layers of a multilayer board is done visually, and human inspectors are—at best—only 90% effective in catching defects in each layer. This means that the overall assurance of quality for, say, a six-layer board is a maximum of 53% (0.9^6). In addition, the complexity of boards is increasing rapidly, with finer line widths and tighter tolerances, so that achieving even 90% accuracy from human inspectors is becoming difficult. Because of these factors, bare PCB inspection is currently a very active area in the machine-vision industry.

Many challenges face the makers of vision systems for this kind of inspection. Properly illuminating the board is the first problem; the system must be able to distinguish traces from substrate. Achieving the needed resolution is another problem. If the field of view is 1/2" square and the vision system has a spatial resolution of 512 × 512, then one pixel corresponds to approximately 1 mil (0.001"). If the board is 40" square (not very big) and the desired resolution is 1 mil, then 160 separate views (images) of the board will be necessary. Further, if the analysis of each image takes one second, then a complete board inspection will require over two and a half minutes. Clearly, inspection of bare boards at production rates is a formidable task.

Loaded or stuffed PCBs also require visual inspection, both top and bottom. Top-side inspection checks for the presence or absence of parts, the correctness of parts, and part orientation (polarity). As with bare boards, a number of images may be needed to complete a single board inspection. However, because the resolution needed is generally not as fine as for bare-board inspection, fewer images are required and faster throughput is possible.

Bottom-side inspection of stuffed PCBs is needed during two stages of the production process. Prior to wave-soldering, a vision system can be used to insure that component pins have been correctly inserted, and to reject boards with bent or missing pins. After soldering, the system can inspect for proper solder coverage including shorts, bridges and incomplete coverage. These inspection tasks are particularly difficult for human inspectors, but with good lighting can be relatively easy for machine-vision systems.

OPTICAL CHARACTER RECOGNITION

Another application for machine vision in the electronics industry is optical character recognition (OCR). There are many uses for OCR during electronic manufacturing, some of which were touched on earlier in this article. For example, information etched on wafers and dice can be read with machine-vision systems. Also, character verifiers can be used to check the brands on IC packages before the ink is set, insuring that each brand is correct, complete, and properly positioned.

A more complicated application for OCR arises during the testing procedure for high-performance ICs. Each part is marked with a unique serial number. As the part is cycled through various environmental and electrical tests, its serial number is read and test results are carefully recorded. With the use of a machine-vision system, it is possible to completely automate the demanding record-keeping chores associated with the testing of high-grade commercial and military parts.

OTHER APPLICATIONS

Other electronics manufacturers, besides those making components or board-level products, want to use machine vision. Producers of floppy disks, for example, need to inspect the disks for cosmetic defects. Although smudges or marks on a disk do not necessarily affect performance, they can cause concern to customers. Therefore, producers want to make sure they ship disks which look perfect.

Keyboard manufacturers are another group interested in cosmetics. They need to insure that all keys have the right characters in the proper position and printed in the correct color and intensity. The shape of the keyboard and keys (keys in different rows differ in shape and orientation) are also features of interest; due to the three-dimensional nature of the parts, variations of lighting and focus make this inspection task a particularly difficult one.

Finally, some electronic products, such as disk drives, have mechanical parts which must be inspected before or after assembly. As production volume of these products increases, manufacturers are more and more interested in automating the inspection process. Machine vision is likely to have an expanding role in this area also.

CONCLUSION

Although electronics is but one of many industries where machine vision can aid the transition to the flexibly automated factory, it offers a particularly wide range of attractive applications; the IVS-100 series from Analog Devices has been designed to make a major contribution to this market. Our powerful hardware and machine-vision software, as well as applications packages currently under development, will help solve many challenging problems facing manufacturers of electronic parts, processes, circuits and systems.

MACHINE VISION AT ANALOG DEVICES

Identifying and developing promising new products is a critically important and exciting task at Analog Devices. After two years of research and development, the market for factory automation is being addressed by "THE EYE," the trademarked name for an intelligent vision-system being marketed by the Machine Vision Products Group (MVP). The story of how this opportunity was developed is in many ways typical of how entrepreneurial ventures are nurtured at Analog Devices.

Before the initial design for "THE EYE" was developed, an extensive market investigation was performed in order to understand the kinds of problems key end-users were experiencing in the area of machine vision. Thorough market analysis is typically the start of product development at Analog. The analysis included users and leading technical experts in the field.

A critical goal of the research was determining the software needs for handling sophisticated industrial vision applications. The intention was to design the hardware for the new system to process efficiently the kinds of vision algorithms required for industrial image analysis. An important finding justified a departure from the basic binary (i.e., black-and-white) algorithms, typical of first-generation industrial vision systems. The new system would be designed to be a balanced package, capable of efficiently executing vision algorithms, yet handling a variety of real-world machine-vision problems.

The machine-vision group drew heavily upon ADI's expertise in video data-acquisition and digital signal processing. The experience of Analog's Measurement and Control Division (MCD) in building integrated factory-automation computers greatly supported the machine-vision effort. A team of vision experts, many with strong experience in medical image processing, joined the team. Important relationships were developed with vision and artificial-intelligence scientists at several universities, including Brown, New York University, and MIT. The strong foundation of MCD's manufacturing and test facilities and field-service organization further aided the machine-vision product commercialization process. Finally, in June, 1984, MVP's first product, the IVS-100, was announced.

The IVS-100 serves both as a development system and as a target unit for solving particular vision applications. It features 256 gray-scale processing, a triple-processor architecture, which relieves the CPU from performing I/O and mathematical tasks, and the latest in microprocessors, Intel's 80186, 80286, and 80287. These features result in a high-performance vision system able to make accurate, high-speed analyses. Important initial markets for the IVS-100 include inspection applications in the electronic, electrical, automotive, and aerospace industries, and interfacing with robots for part location and in assembly operations.

MONOLITHIC ANALOG TRIGONOMETRIC FUNCTION GENERATOR

AD639 Computes SIN, COS, TAN, Plus Reciprocal, Inverse, and Offset Functions Complete and Self-Contained; SINE and COSINE Accuracy Specified over ±360°

by Barrie Gilbert

The AD639* is an analog "trigonometric microsystem" on a single silicon chip, packaged in a 16-pin DIP. From a differential voltage input, representing an angle, (20 mV/°), it can be pin-programmed to generate a voltage output, accurately determined by any of the standard functions—sine, cosine, tangent, secant, cosecant, and cotangent—as well as some lesser-known variants, such as the versine and exsecant, plus a corresponding set of inverse functions. All inputs are differential, and either polarity of input or output can be accepted or generated.

Figure 1 shows the sinusoidal output-vs.-input characteristic of an AD639 when driven over (and beyond) the ±540° range of the *x*-input angle. Smooth and differentiable, the function is laser-trimmed to maintain good law-conformance over this range, with a typical mismatch in its six peaks of only 0.05%. The "B" grade is specified to have an absolute accuracy to within 0.8% of full-scale output for a 10-volt sine from −180° to +180° of angular input and a −25°C to +85°C operating temperature range. The output bandwidth is 1.5 MHz. Prices start at $12 in 100s ("A" grade).

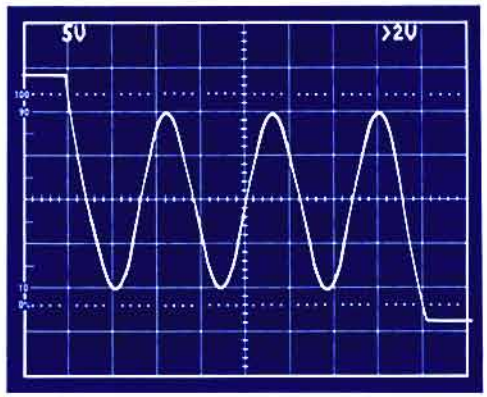


Figure 1. The AD639's voltage output vs. its X-angle voltage input. Each 90° interval is 1.8 volts of input. Total range is over 1000°.

WHAT IT'S USED FOR

Trigonometric functions play an important role in electronics. Inherent to many communications, measurement, and display systems, they also find increasing application in control and robotics.

Most familiar are the *sine* and the *cosine*, which find wide use as fundamental signal sources—both separately and in orthogonal pairs. In display systems, these functions are basic to graphical manipulations (axis rotation and polar-to-Cartesian conversion), and they also appear in many antenna-related signal transformations. The *tangent* is important in scanning systems, and the *arctangent* is used in Cartesian-to-polar conversion and in determining phase angle from the real and imaginary components of a complex signal. The AD639 is equally adept in all these modes, and more.

WHY THE AD639?

Until now, there has never been a fast, accurate, general-purpose analog trigonometric function generator available in a compact, low-cost form, such as a monolithic IC. In the past, *analog* approaches were either fairly accurate but complex and slow, typically making use of polynomial synthesis or large piecewise-linear networks—or comprised simple but inaccurate and temperature-prone circuits, directly employing nonlinearities of diodes and transistors. *Digital* approaches, on the other hand—employing lookup tables in ROM and counters, or numerical algorithms on a microprocessor—can be accurate, but only when using high-resolution DACs and often much additional circuitry, and the final output frequency is often limited to a few hundred hertz.

The versatile, easily used AD639, with its large repertoire of functions, makes it possible to include trigonometric transformations in the analog portion of a system with little added cost or board space, and with high accuracy, without the overhead in software, memory, or time which would accompany such computations in an associated digital system. It also makes it easy to generate low-distortion sine-wave signals, with voltage control of amplitude and frequency, up to 10 V and 1 MHz respectively.

WHAT IT IS AND DOES[1]

Figure 2 is a combined block diagram and pinout of the AD639. There are four sets of differential voltage inputs (U, X, Y, and Z) and a control input, UP. The main output, W, is a loadable voltage of ±10V full scale; there is also a reference voltage, VR, of +1.8 volts, which corresponds to 90°. A dual-purpose pin, GT, can be used as a gating input or to provide an output indicating an error condition.

The heart of the AD639 is a pair of sine-synthesis networks which

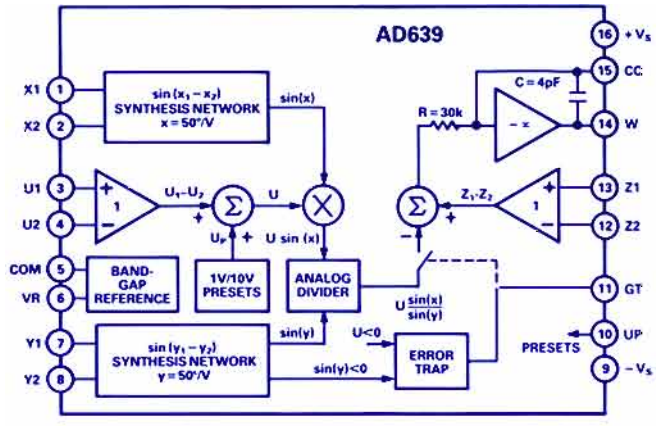


Figure 2. Functional schematic of the AD639.

[1] For details of the sine networks, see:
Barrie Gilbert, "A Monolithic Microsystem for Analog Synthesis of Trigonometric Functions and their Inverses," *IEEE Journal of Solid-State Circuits* SC-17 no. 6 (December 1982).
Barrie Gilbert, "A Remarkable Monolithic Microsystem Generates Trigonometric Functions," *Industrial Electronics Equipment Design* (15 September 1984).

*Use the reply card for technical data.

generate internal signals, both accurately proportional to the sines of angles x and y, which are in proportion to voltage inputs X and Y—with a scaling factor of 20 mV/°:

$$\sin(x_1 - x_2) = \sin \frac{X_1 - X_2}{1.8\,V} \cdot \frac{\pi}{2} = \sin \frac{X_1 - X_2}{1.8\,V}\ 90° \qquad (1)$$

$$\sin(y_1 - y_2) = \sin \frac{Y_1 - Y_2}{1.8\,V} \cdot \frac{\pi}{2} = \sin \frac{Y_1 - Y_2}{1.8\,V}\ 90° \qquad (2)$$

The sines are generated by similar networks, but they have different usable input ranges; x has a range exceeding ±500°, but the design requires that only the 0° to +180° portion of the y range be used. The sin x and sin y terms are then divided to form a ratio, and multiplied by voltage, U, equal to $U_1 - U_2 + U_P$. (The multiplication and division are an implicit part of the integrated design, but the functionality is most readily grasped using the explicit form shown in Figure 2.) U is the amplitude-control voltage; the differential input, $U_1 - U_2$, provides external, variable control, with a gain of unity to the output, while U_P provides a convenient fixed amplitude of either +1 V or +10 V, by taking UP (pin 10) to a voltage either above or below ground (usually to $+V_s$ or $-V_s$). The variable and fixed amplitudes can be used in combination for modulation. The resulting signal is applied to the inverting output of the output op amp, which has a closed-loop bandwidth of 1.5 MHz. Feedback around this amplifier is via a further differential interface, Z.

For direct functions (such as the sine), Z1 is connected to the output, W, and Z2 is grounded. (Z2 may be used to sum a further input, if desired, or in a variety of other ways). The output is then simply the ratio of the sines of angles x and y, multiplied by the voltage, U. If either y or U becomes negative—a condition leading to gross errors—the integral error-trap will switch the output to zero (or to the voltage on Z2) and GT (pin 11) goes high. This can be disabled by grounding GT; alternatively, the GT pin can be used to force the output off at any time, for example, for sine-burst generation.

In general, the AD639 has the following transfer function:

$$W = A_0\left[(U_1 - U_2)\frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)} - (Z_1 - Z_2)\right] \qquad (3)$$

To clarify the explanation of how the circuit can work in other modes, the preset amplitude, U_p, is omitted here. A_o is the open-loop dc gain of the op amp and is very high. Provided that the resulting circuit is stable, W can be connected back to any of several inputs in such a way that the quantity inside the brackets is forced essentially to zero.

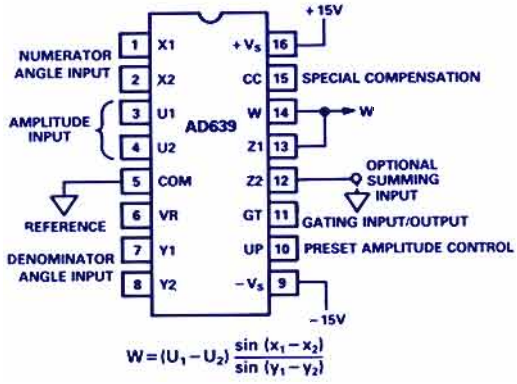


Figure 3. Connections for direct functions, such as sine and tangent.

As a result, the circuit forces a balance between two ratios:

$$\frac{Z_1 - Z_2}{U_1 - U_2} = \frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)} \qquad (4)$$

Using the connections for "direct" functions (Figure 3), we get

$$W = (U_1 - U_2)\frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)} \qquad (5)$$

TRIGONOMETRIC COMPUTATIONS

To generate the sine of a single-ended voltage, X_1, Y1 is connected to VR, which corresponds to 90°, and X2 and Y2 are grounded. Thus, the numerator angle is simply x_1, equal to $(X_1/1.8\ V)\cdot 90°$, and the denominator is sin(90°), or 1. The amplitude can be preset to 10 V by connecting UP to +Vs, and—with U1 and U2 grounded—the output becomes

$$W = 10\,V \sin\left(\frac{X_1}{1.8V}\ 90°\right) \qquad (6)$$

For an output having an inverted polarity, $-\sin x$, which is equal to $\sin(-x)$, it is only necessary to interchange X1 and X2; in fact, all the direct functions can be inverted in this way. For the cosine, use the relationship (see Table 1) $\cos x = \sin(90° - x)$; both X1 and Y1 are connected to VR, Y2 remains grounded, and the input is applied to X2.

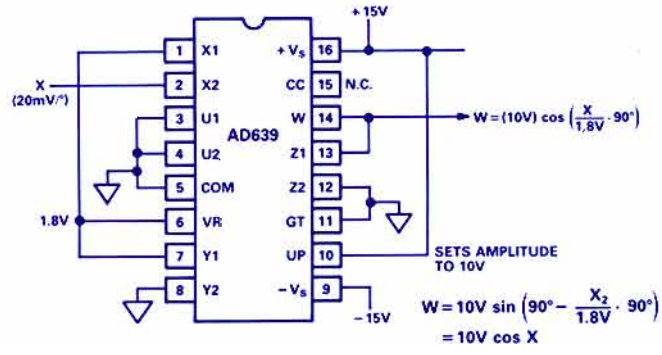


Figure 4. Example of connections for (10 V)cos x.

For the tangent—the ratio of sine to cosine—the device is connected as shown in Figure 5(a) to implement this function:

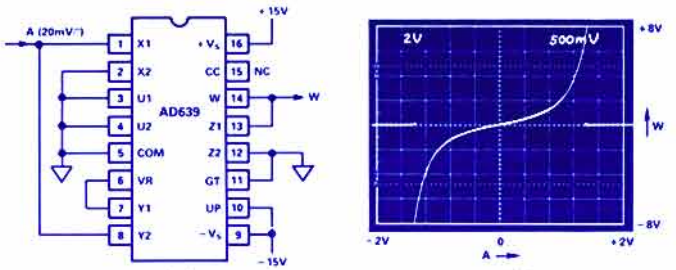
$$W = (1V)\frac{\sin(a - 0°)}{\sin(90° - a)} = (1V)\frac{\sin a}{\cos a} = (1\,V)\tan a \qquad (7)$$

A preset of $U_p = +1V$ is used here to allow processing of angles from −85° to +85°, when the output will be −11.43 V or +11.43 V, respectively. Beyond this range, W exceeds the capability of the output amplifier and is automatically suppressed by the error-trapping circuitry, as shown in Figure 5(b).

All the "direct" functions are easily implemented using the formulas shown in Table 1. Remember that the denominator, y, must be positive; the odd-order symmetry of the sine in the numerator, combined with the availability of differential X inputs, means that

Table 1. Formulas for the Direct Trigonometric Functions

$\sin a = \frac{\sin a}{1} = \frac{\sin(a-0°)}{\sin(90°-0°)}$	$\csc a = \frac{1}{\sin a} = \frac{\sin(90°-0°)}{\sin(a-0°)}$
$\cos a = \frac{\cos a}{1} = \frac{\sin(90°-a)}{\sin(90°-0°)}$	$\sec a = \frac{1}{\cos a} = \frac{\sin(90°-0°)}{\sin(90°-a)}$
$\tan a = \frac{\sin a}{\cos a} = \frac{\sin(a-0°)}{\sin(90°-a)}$	$\cot a = \frac{\cos a}{\sin a} = \frac{\sin(90°-a)}{\sin(a-0°)}$



(a) (b)

Figure 5. Tangent function. (a) Connections. (b) Output vs. input.

the overall sign of any output function can be inverted just by interchanging X1 and X2.

The AD639 can be used to generate less-common functions, such as the coversine of angle a, which is simply $(1 - \sin a)$. This is formed by connecting an amplitude-scaling voltage to both the U1 input and the Z2 input, Z1 to W, X2 to the angle input signal, Y1 to VR, and U1, X1, and Y2 to ground. Now, whatever voltage is applied to U1 appears directly at the output (via Z2) and is summed with $U_1 \sin(-a)$ via the normal path in the AD639. Hence, $W = U_1 (1 - \sin a)$. Other functions, such as the versine, $(1 - \cos x)$, and exsecant, $(\sec x - 1)$, can be generated by similar means.

INVERSE FUNCTIONS

For inverse functions, the output, W, now corresponds to an angle, w. Accordingly, it is generated by forcing the angle input(s) by feedback from the output, until the generated function exactly balances inputs applied to U and Z, that is, by using the balance equation (4). For the arctangent (the most useful function), the connections of Figure 6a are used; then (4) becomes

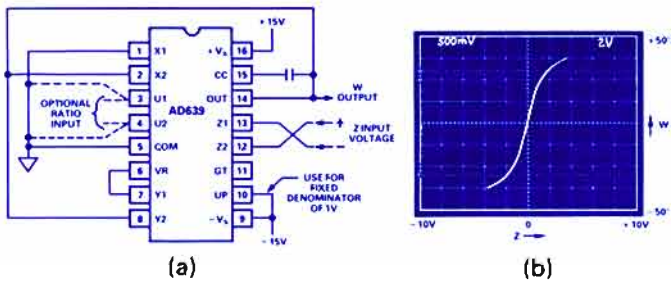
$$\frac{Z_1 - Z_2}{U_1 - U_2} = \frac{\sin(0° - w)}{\sin(90° - w)} = -\tan w \qquad (8)$$

The negative tangent ensures that the overall feedback is negative. Since the closed-loop gain around the op amp can now be much higher than in the direct modes, an additional capacitor, C_C, is needed to keep the loop stable for large values of angle. Rearranging (8),

$$w = \tan^{-1}\left(\frac{Z_2 - Z_1}{U_1 - U_2}\right) \qquad (9)$$

Thus, in its general form, the circuit can actually generate the arctangent of the ratio of two voltage inputs. If, as shown in Figure 6(a), the U-preset is enabled for $U_p = +1V$, the function is the "simple" arctangent

$$W = (1.8V)\frac{\tan^{-1}\left(\frac{Z_2 - Z_1}{1V}\right)}{90°} \qquad (10)$$



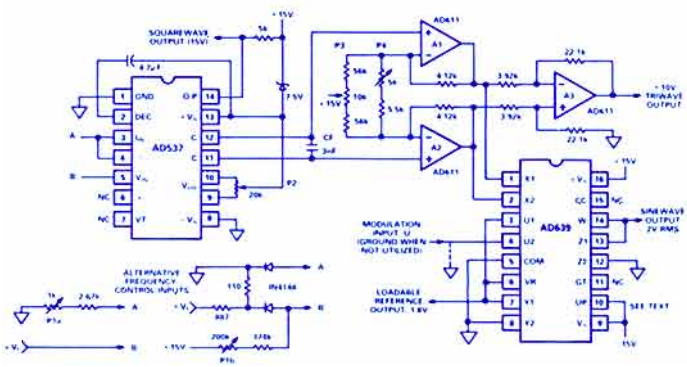
(a) (b)

Figure 6. Arctangent function. (a) Connections. (b) Output vs. input.

Figure 6(b) shows the resulting output for a range of ±75°. In practice, suitable precautions must be taken to prevent the equivalent angle, w, from exceeding ±90°, which could cause the output to "solve" for a value outside of the principal range.

A COMPLETE FUNCTION GENERATOR

As an example of the utility of the AD639 as a function generator, Figure 7 shows a complete, low-cost circuit which provides sine, square, and triwave outputs, with voltage-control of frequency, from 20 Hz to 20 kHz, and a preset sine amplitude of 2.8 V (within 0.1 dB of 2 V rms), which can be modulated by applying a voltage of up to ±2.8 V to U2, or gated by applying a TTL input to GT. For 10-volt output amplitude, the 10-V preset is used with U1 grounded.



(a) Linear Input (b) Log/Exp Input

Figure 7. Function generator with voltage-programmable frequency and nominal 2-V rms sine amplitude which can be modulated using U input.

An AD537 V/F converter is used to generate the triwave—which appears across the timing capacitor, C_t. After level-shifting and amplification by A1 and A2, the triwave is applied to the AD639, for an input range of −90° to +90° in the sine mode. A3 provides further gain, for a ±10-volt triwave output. The square-wave output is taken directly from the AD537 and is unbuffered. As shown, it swings between ground and +15 V; if pins 1 and 8 of the AD537 are connected to −15 V, this output is 20 volts peak-to-peak.

Alternative input networks are suggested for controlling frequency. Inset (a) shows a linear interface, with 10kHz/V scaling, calibrated with P1a. The maximum input is +2V (f_{max} = 20 kHz). To maintain frequency accurately for small inputs, the V_{os} of the AD537 must be nulled, using P2. The frequency may be controlled manually, by deriving a voltage from the AD639's +1.8-volt reference, using a potentiometer; P1a has sufficient range to allow a full-scale frequency of 20 kHz, and P2 is not needed in this case.

The network shown in inset (b) provides a "log-sweep" input, with the approximate scaling,

$$f = 10^{V_f}\ \text{kHz}\ (V_f \text{ in volts}) \qquad (11)$$

The range in this case is from about 10 Hz to 100 kHz; P1b and P2 should be adjusted for f = 100 kHz at V_f = +2 V, and f = 100 Hz at V_f = −2 V. The frequency here is sensitive to variations in both temperature and supply voltage, but this network is still useful in non-critical cases because of its simplicity.

P3 and P4 are adjusted using a spectrum analyzer; P3 minimizes second-harmonic distortion and P4 minimizes third harmonic. Distortion cannot be reduced to the degree the AD639 is capable of, due to the relatively poor quality of the triwave.

MONOLITHIC SAMPLE-HOLD IS COMPLETE, FAST, ACCURATE

AD585 Has On-Board Capacitor and Gain Resistors, 12-bit Linearity, Low Error Up to 78-kHz 12-Bit Sampling; Only 0.6° Phase Shift for 20-kHz Signals

by John Croteau

The AD585* is a monolithic sample-hold amplifier (SHA) housed in a 14-pin CER-DIP package. Complete on one chip, it includes an internal 100-pF *hold* capacitor with dielectric absorption of the order of 0.01%—and a set of on-chip precision gain resistors for choosing pin-programmable gains of +1, +2, or −1.

Near-ideal for designs with the 12-bit AD574A a/d converter (or competitive clones), its principal specifications include a fast 3-μs acquisition time to 0.01% (max) for 10-volt steps, low droop rate of 1 mV/ms (max), a trimmable sample-hold offset step of 3 mV (max), and 0.5-nanosecond aperture jitter. Two versions are available, AD585AQ (−25°C to +85°C) and AD585SQ (−55°C to +125°C). Prices (100s) are $9.90 and $38.70.

BACKGROUND

The emergence of microprocessor- and microcomputer-based data-acquisition systems during the past decade has fostered advances in the resolution, accuracy, and throughput of integrated-circuit a/d and d/a converters. Today, successive-approximation ADCs in monolithic and multi-chip form provide up to 12-bit performance at a fraction of the cost of the older hybrids, modules, and pioneering ICs. To accompany them, there is an increased need for fast, accurate sample-hold functions to allow signals having reasonably wide bandwidths† to be converted with comparable resolution and accuracy - at low cost.

Unfortunately, the development of the sample-hold amplifier as an IC support component has lagged that of the a/d converter in technology, design, and performance—and with good reason; a high-performance sample-hold is one of the most-challenging of analog circuits to design. Until recently, the circuit or system designer has had to make a difficult choice between an expensive module or hybrid, a suitable—but expensive—home-grown design, or a low-cost IC with marginal specifications (and perhaps even worse performance).

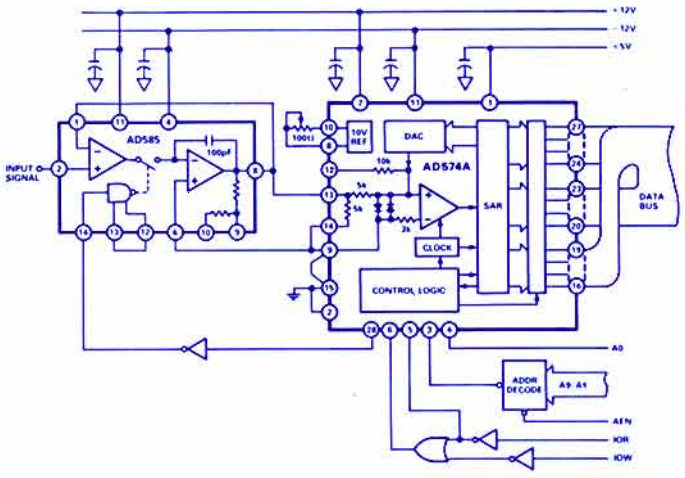


Figure 1. The AD585 sample-hold, used with the AD574A 12-bit ADC.

*For technical data, use the reply card.

†For information about why sample/track-holds permit faster sampling with ADC's—even "flash" ADCs—see "Flash Converters Work Better with Track-Holds," by Jerry Neal and Jim Surber, *Analog Dialogue* 18-2 (1984), 10-14.

USING THE AD585

The AD585 is a definitive solution to the general-purpose 12-bit design problem, especially when used in conjunction with the AD574A a/d converter. In Figure 1, the pair forms an analog input port for an IBM PC-based measurement-and-control system.

Without a sample-hold, the input sampling period is 35 μs, the AD574A's conversion time. For less than ½ LSB change during sampling, the highest signal-frequency for ½-LSB error would be

$$f_{max|12\,bits} = \frac{2^{-(n+1)}}{\pi \cdot 35 \times 10^{-6}}$$

$$= 1.11\ \text{Hz}$$

As a front-end for the AD574A, the AD585, with its aperture-jitter spec of 0.5 ns, increases the maximum frequency for ½-LSB sampling by a factor of 35,000/0.5, or 70,000, to 78 kHz. But the practical limit to the sampling frequency is the reciprocal of the sum of the conversion time (35 μs) and the AD585's acquisition time (3 μs), or 26.3 kHz. Thus, the maximum signal frequency that can be handled by the AD585/AD574A combination (as dictated by the Nyquist criterion), is 13.1 kHz, a ten-thousandfold improvement over the AD574A by itself. When the AD585 is used with 12-bit converters having shorter conversion time—for example, 10 μs—the maximum signal frequency increases towards 38 kHz.

While doing its job of reducing dynamic errors, a SHA should avoid introducing substantial amounts of other kinds of error. The AD585 provides excellent all-around performance. For example, the AD585's 100-pF hold capacitor is small enough to permit slewing at 10 V/μs and acquisition to 0.01% in 5 μs max for 20-V steps, yet large enough to limit droop to 1 mV/ms (max) with the 100 pA of leakage current. Switch charge-transfer produces a trimmable 3-mV sample-to-hold offset, which varies by only 300 μV over a 20-volt range (extremely low dynamic nonlinearity).

Finally, a sample-hold must be capable of low output-voltage error and rapid recovery in the presence of large, fast current pulses, such as are found at the inputs of many successive-approximation ADCs during conversion. Figure 2 compares the outputs of an AD585 and a popular sample-hold IC under those conditions.

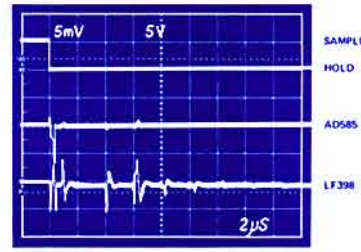


Figure 2. Output of the AD585 when driving a successive-approximation converter – compared with a popular IC SHA.

RESOLVER/DIGITAL WITH ACCURATE TACHOMETRIC OUTPUT

New Hybrid Converters Offer 10-, 12-, 14-, 16-Bit, or Variable Resolution For Brushless Tachometry, Numerical Control, Feedforward Stabilizing, etc.

by Paul Nickson and Geoffrey Boyes

The 1S14, 1S24, 1S44, & 1S64*, and the 1S74*, (known generically as 1Sn4's) are a pin-compatible family of hybrid-circuit resolver-to-digital converters (RDCs), in 40-pin packages, designed for applications that call for both accurate digital position information and an output voltage accurately proportional to shaft velocity, in data acquisition employing Inductosyns™ and resolvers.

The 1S14/24/44/64 have fixed resolutions of 10/12/14/16 bits, and inversely related maximum speeds, as indicated in Table 1; the 1S74 has a choice among all four digital resolutions, as determined by permutation of the logic applied to a pair of resolution-select terminals. Since resolution and maximum speed are inversely related, a single 1S74 unit can be digitally programmed for range-switching to handle applications with a wide range of speeds.

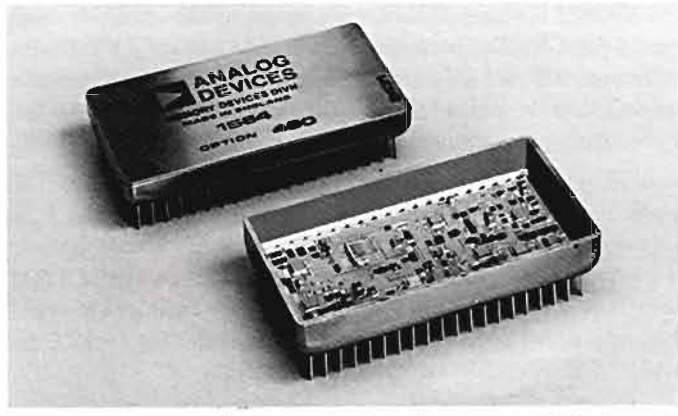
Table 1. Comparative performance of 1Sn4 converters.

TYPE	POSITION SPECS		SPEED SPECS	
	Angular Resolution (Bits)	Accuracy Error (arc-min)	Tach Sensitivity (V/krpm)	Max Speed (rpm)
1S14	10	±25	0.25	40,800
1S24	12	±8.5	1.0	10,200
1S44	14	±5.3	4.0	2,550
1S64	16	±4	16.0	630
1S74	10-12-14-16, Digitally set	Specs depend on resolution, as above		

WHY ACCURATE TACHOMETRIC OUTPUTS?

Tachometric outputs provide voltage proportional to rotational speed. In servo systems, there are two basic reasons for speed measurement, and electromechanical tach generators have traditionally served to satisfy both requirements:

The most usual application is in stabilization, or damping, of servo



systems; since speed is proportional to the rate at which the position error is changing, it provides an anticipatory control term, which improves speed and stability of a servo loop. This is not a demanding requirement, and a low-grade tachometer (one having not particularly good ripple, linearity, and scaling accuracy) will perform adequately—if it has low inertia and wide dynamic range.

The other application is for accurate speed control in velocity servos; typical uses include synchronizing rollers in paper and printing machines, and for generating accurate velocity profiles in machine tools and robots. For this form of application, high-grade (i.e., expensive) tachometers, having low ripple and nonlinearity—and good performance at very low speeds—are needed.

The important—and indeed fortunate—aspect of the increasing tendency to join reliable brushless resolvers with compact, low-cost hybrid resolver-to-digital converters in systems for position measurement is this: the conversion method employed—the Type 2 tracking loop—provides an inherent (i.e., *free*) analog measure of speed, which makes it possible to eliminate tachometers. This can be seen in Figure 1, the functional block diagram of the tracking loop employed for the 1Sn4 series.

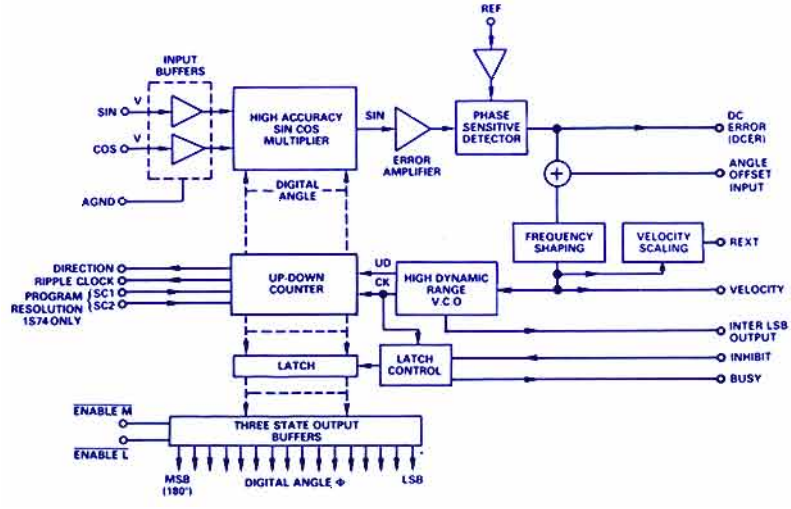


Figure 1. Functional diagram of resolver-to-digital converter.

*Use the reply card for technical data.

™Inductosyn is a registered trade mark of Farrand Controls, Inc.

While this architecture has been used in earlier designs (for example, the 1Sn0 series, described in the last issue of *Analog Dialogue* (18-2, page 22), not much attention was paid to optimizing the velocity output, since the velocity output didn't have to be exceptionally accurate in order to build RDCs having excellent position accuracy and dynamic performance. However, as a result of concentration on this aspect of the design, the 1Sn4 series, for the first time in the industry, makes available *both* a high-performance velocity output with up to 100-dB dynamic range, 0.1% linearity spec, and 0.5% ripple, for cost-effective replacement of tach generators, and a choice of position resolutions up to 16 bits.

HOW IT WORKS

A brushless resolver (Figure 2) has two stator windings, at 90° to one another. A rotor winding is energized with an ac *reference* signal, at frequencies up to 10 kHz; it induces voltages in the stator windings, proportional to the sine and cosine of the shaft angle. The reference voltage is coupled to the rotor from a separate stator winding, via a rotating transformer, which eliminates brushes and slip-rings.

The stator outputs, A sin ωt sin θ and A sin ωt cos θ (θ is the shaft angle), connected to the inputs of the RDC, are multiplied by the sine and cosine of a trial angle, ϕ, stored in a digital register, giving:

$$A \sin \omega t \sin \theta \cos \phi$$
$$A \sin \omega t \cos \theta \sin \phi$$

and subtracted, to obtain an ac voltage proportional to the sine of the difference between θ and ϕ, i.e., the error of ϕ:

$$A \sin \omega t \sin (\theta - \phi)$$

The error signal is demodulated in a phase-sensitive detector, filtered, and applied to the input of a wide-dynamic-range voltage-controlled oscillator (VCO). The output of the VCO drives an up-down counter in the appropriate direction for the loop to cause its output, ϕ, to home in on—i.e., *track*—the value of θ, ideally bringing the position error to zero, within 1 LSB. (An auxiliary incremental analog position output permits a further increase of fine structure by interpolation within 1 LSB.) Since the rate of counting is proportional to the VCO input, and the accumulated count is equal to the angle, ϕ, the input to the VCO is proportional to the rate-of-change of ϕ, hence the velocity, $d\phi/dt$. As ϕ tracks the input angle, θ, the VCO input becomes proportional to $d\theta/dt$.

It's worth noting that, since an Inductosyn is essentially a flat resolver, with ac excitation applied to the stationary winding pattern—and outputs taken from two 90°-phased windings on the slider, the RDC can be used with it to measure position and speed in the same way, with the amplified slider signals as inputs. In both cases, additional counters can be employed to get measurements of absolute position, as the resolver makes complete rotations, or the Inductosyn slider encounters each cycle of the stationary pattern. For this purpose, the *pitch counter* terminals provide pulse (ripple clock—RC) and direction (DIR) information to an up/down counter.

FEATURES

Connections to the 1Sn4 series RDCs are typefied by the circuit of Figure 3. Three-state digital outputs (*output angle*) and 2-byte output word permit interfacing to 8- or 16-bit buses, using the *data-transfer* control terminals. Typical resolver connections (*sine*, *cosine*, and *reference*) are shown at the lower left. DC *power* ($+V_S$, $-V_S$, and $+5V$) is furnished at lower right.

The *tacho output* terminal provides a dc voltage, scaled to speed, as shown in Table 1. The *inter LSB* terminal provides an analog interpolation signal, representing resolver shaft position at the LSB level, to overcome the inherent "free play" in a servo system using digitized position feedback. The *angle offset* input permits the user (in effect) to rotate the input shaft of the resolver electrically by up to 30 LSB, using an externally generated current. The *REXT* terminal permits an external resistor, connected to ground, to increase the tachometer sensitivity (V/krpm) above that specified in Table 1.

Finally, the *DC error* terminal makes available the phase-sensitive detector's output; it is proportional to the error between the input angle and the digital output angle. Normally very close to zero, this error increases transiently on sudden changes in loading or speed; the error is sustained if the output fails to track the input, either because the input has exceeded the maximum tracking rate of the converter, or (because of a malfunction) the converter is unable to reach a null. With an external window comparator (pair of comparators), this voltage can provide a built-in test (BIT). ■

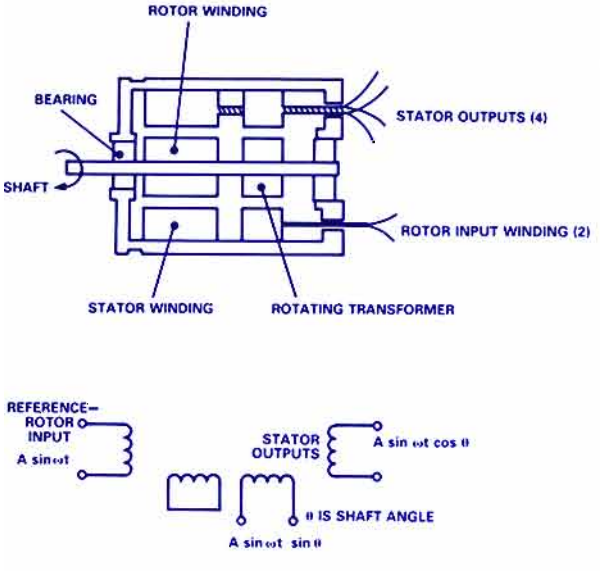


Figure 2. Brushless resolver construction.

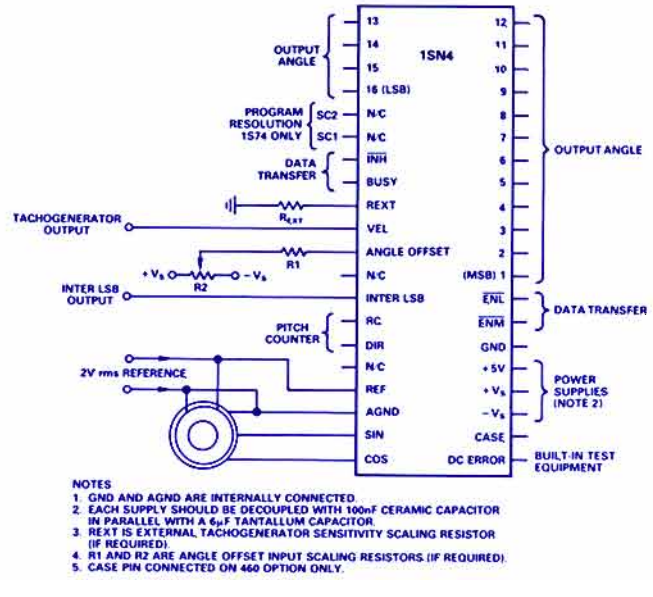


Figure 3. Electrical connections.

FAST 1.5-MICRON MULTIPLIER & MULTIPLIER/ACCUMULATORS

Advanced CMOS Process for High Speed and Low Dissipation in 3 New DSP Chips

Example: ADSP-1010AK 16×16 MAC Has 95 ns max Cycle Time, 200 mW max Dissipation

Analog Devices has just introduced three new CMOS integrated circuits for digital signal-processing (DSP), the ADSP-1010A 16 × 16-bit Multiplier/Accumulator (MAC), the ADSP-1016A 16 × 16 Multiplier, and the ADSP-1008A 8 × 8 MAC.* (Three additional devices, the ADSP-1009A, ADSP-10012A, and ADSP-1080A are waiting in the wings; they will be introduced shortly.)

Fabricated with an improved proprietary 1.5-micron process, they are the first in a new series designed to replace earlier ADSP models (without the "A" suffix), while providing more than twice the specified speed of the corresponding devices. In addition, besides retaining the CMOS advantage of much lower dissipation than equivalent industry-standard bipolar devices (TDC1010J, MPY-16J1, and TDC1008J4), they are also considerably *faster*.

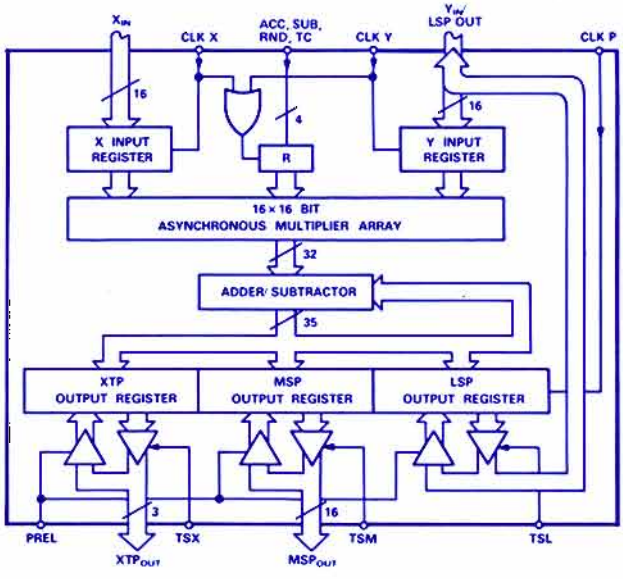


Figure 1. Block diagram of ADSP-1010A 16 × 16 Multiplier-Accumulator.

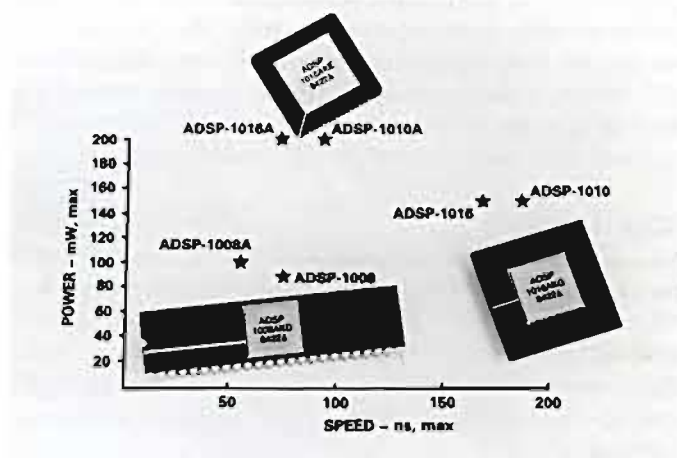
Table 1 compares the new devices with their earlier CMOS progenitors. It should be noted that the specified cycle times and dissipations for all Analog Devices CMOS DSP components are maximum over the specified *ambient* free-air temperature range (not case temperatures). The reason is, unlike bipolar types, these

Table 1. Selection chart and performance comparison, 5 μm vs. 1.5-μm geometries

Type	Device	Resolution	Cycle Time# (ns)	Dissipation# (mW)	Process (μm)
ADSP-1008	MAC	8 × 8	125	75	5
ADSP-1008A	MAC	8 × 8	55	100	1.5
ADSP-1016	MULT.	16 × 16	170	150	5
ADSP-1016A	MULT.	16 × 16	75	200	1.5
ADSP-1010	MAC	16 × 16	190	150	5
ADSP-1010A	MAC	16 × 16	95	200	1.5

Note: Highest grade, max over rated *ambient* temperature.

*For technical data, use the reply card.



CMOS devices have little internal temperature rise—not enough to reduce the specified ambient operating temperature range. This factor is especially important for devices that must operate over the full military ambient temperature range, −55°C to +125°C.

The net result is that DSP system designers can now attain high throughput, using these form- and function-compatible devices, while avoiding the penalties associated with high power dissipation in the fast bipolar and NMOS implementations of the industry-standard architectures.

In addition to the high speed inherent with small 1.5-micron geometries, the speed of the devices is further enhanced by the use of a modified Booth algorithm, feed-forward carry organization, and a conditional-sum adder in the final adder stage.

Both 16 × 16 models are available in leadless chip carriers (LCC) and pin-grid arrays (PGA), as well as standard 64-pin DIP packages, affording designers the flexibility needed to suit a variety of system packaging needs. The low dissipation also reduces heat-sink and system cooling requirements.

All three devices are available in grades that include processing according to military standards, as well as lower-cost grades that have only slightly less speed than the highest-speed "K" grade. Prices in 100s (K, in ceramic DIP packages), are $85, $125, and $190, for the ADSP-1008A, ADSP-1016A, and ADSP-1010A, respectively.

APPLICATIONS

These multipliers and multiplier/accumulators may be used in both dedicated computer applications and to augment general-purpose computer-system designs,—in short—wherever digital signal processing can provide enhanced computing power, improve system speed by offloading CPUs, and reduce the software burden by substituting fast, reliable hardware for lengthy software routines.

Typical applications include digital filtering, array-processor design, correlation, image processing, etc. Because of their low dissipation, these devices are especially useful in upgrading performance or reliability of existing system-designs that employ large numbers of multipliers to achieve the benefits of extended parallel processing.

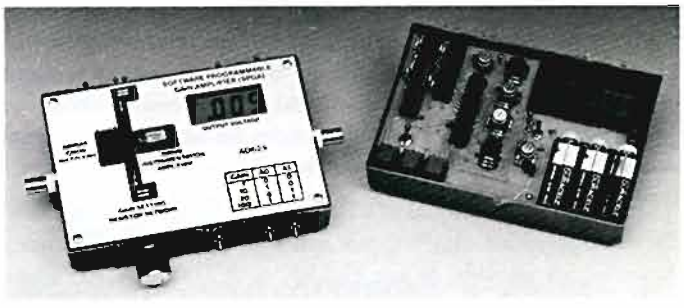
PRECISION DEMO UNITS SIMPLIFY ANALOG IC EVALUATIONS

Demonstration Boxes Put ICs through Their Paces: Thermocouple Measurements, Instrumentation Amplifiers, Wideband Analog Multipliers, Quad D/A Converters

by James Bryant

Analog Devices Applications Engineers have developed for our sales enginers several self-contained battery-operated demonstrators for:

- AD594* Thermocouple Preamplifier
- AD625* Programmable-Gain Instrumentation Amplifier
- AD524* Precision Instrumentation Amplifier
- AD539* Wideband Dual-Channel Analog Multiplier/ Divider
- AD7226* Four-Channel D/A Converter



The photo shows two demonstrators:† At right, the AD7226 quad d/a converter is used for "potless" adjustment of op-amp offsets in four amplifier channels, with resolution of 1 μV; in the other, the AD625 instrumentation amplifier has 2-bit digitally programmed gain, and amplifies a (user-)variable dc signal for DPM readout.

The schematic of Figure 1 illustrates a system, including signal leads, designed to simplify evaluation of the AD524 instrumentation amplifier (Figure 1). A small plastic box, like the ones in the photograph, houses the AD524 and all components, including a shield driver and a ±9-volt battery power supply.

Instrumentation amplifiers—dc amplifiers with high-impedance differential inputs—amplify or buffer differential signals or single-ended signals having a poor-quality ground. These amplifiers have single-ended output, high common-mode rejection ratio (CMRR), and stable well-defined gain, generally in the range 1 to 1000 over a moderate bandwidth.

The AD524 (*Analog Dialogue* 16-3), a high-performance monolithic instrumentation amplifier, requires no external resistors for a choice of gains (1, 10, 100, 1 000), set by jumper connections.

The demo circuit (Figure 1), is quite simple. Besides the AD524, it contains pre-adjusted potentiometers for fine-trimming the output and input offsets, a gain-setting switch, a power switch, and a shield driver, comprising a dual operational amplifier and associated components. (For many fixed-gain real-world applications, *none* of these additional components is necessary).

In use, the signal is connected to the inputs, the switch sets the gain, and the output appears between common and the output terminal. Though negligible, input bias current needs a return path; it is usually sufficient to connect "ground" of the circuit to "ground" of the box, i.e., the midpoint of the AD524's supply.

Demonstrations are usually conducted with an oscilloscope, which displays amplified differential signals, from dc to about 50 kHz. With scope sensitivities of 2 or 5 mV/cm, a gain of 1000 allows signals as small as a few μV to be examined; this is useful (among other things) for measurements of noise and ground-loop voltage in ground conductors. For a convincing demonstration, short-circuit an audio signal generator's output with a piece of wire, and connect probes from the box to the wire—about 2 cm apart (Figure 2).

An IA's excellent CMR can be corrupted by circuit unbalances. For example, the differing phase shifts of two shielded test leads with different source resistances, and shunted by different values of stray capacitance, can introduce a dynamic common-mode error.

To minimize these effects, the stray capacitance is reduced by driving the shields at the same voltage as the signal, greatly reducing the capacitive effect. The gain-resistor terminals, at the same voltage (dynamically) as the input, can be used for this purpose—buffered by a pair of followers (a dual FET-input op amp). ■

*Use the reply card for technical data.
†For a demonstration, get in touch with ADI Component Sales.

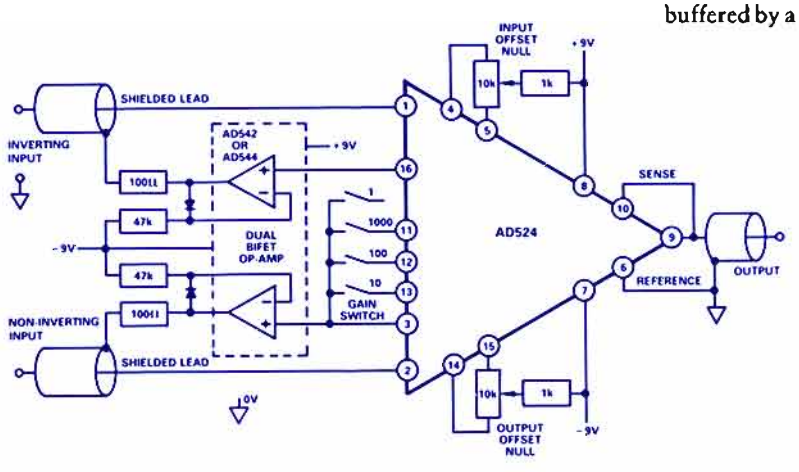


Figure 1. Circuit diagram of demonstration box.

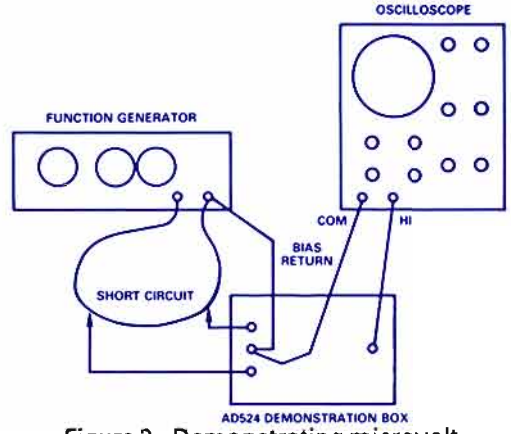


Figure 2. Demonstrating microvolt ground measurements.

8 NEW PLUGIN SIGNAL-CONDITIONING MODULES IN 3B SERIES

Strain-Gage Conditioners, 1500-V Isolated DC, AC, and Frequency Measurements

The 3B Series Multichannel Signal-Conditioning Input/Output Subsystem and modular signal-conditioning plugins* were introduced in these pages two years ago (*Analog Dialogue* 16-3, pp. 7-9). They feature standard output levels, direct connection to sensors, mix-match interchangeable functions, a series of isolated plugins with 1,500-volt isolation, and simultaneous current and voltage outputs to permit both remote transmission and local monitoring of amplified input signals.

The 3B Subsystem consists of a 19" universal backplane and a family of color-coded plugin input and output signal-conditioning modules, all identical in size (3.150" × 0.775" × 3.395") and having the same pin-connection pattern. Besides the 16-channel rack-mountable system depicted at the bottom of the page, self-powered 8- and 4-channel backplanes are also available for decentralized or smaller systems. The modules' protective plastic shells contain provisions for tool-free latching to to the backplane.

The purpose of the 3B is to make available protected general-purpose multi-channel signal conditioning at low cost for safely interfacing input and output transducers in the field to data-acquisition or control systems at standard voltage and current levels. Because the concept has been so successful, a wide range of new plugins is now introduced to provide more options for users.

THE NEW INPUT MODULES IN BRIEF

Table 1 lists all of the available *input* modules. Four categories of newly introduced modules are identified by boldface type:

- **Strain-gage conditioners** (3B18)* provide excitation and amplification for bridges with impedances from 100 ohms to 10 kΩ. Excitation is +3.3 V or +10.0 V, switch-selectable, and bandwidth is 20 kHz. Each 3B18, calibrated to within 0.1%, offers low drift, high noise rejection, and 130-V rms input protection.

- **Wideband dc signal conditioners** (3B40 and 3B41)* provide amplification of dc-to-10-kHz signals. The low-level 3B40 accepts full-scale input signal ranges from ±10 mV to ±100 mV, and the 3B41 has full-scale ranges from ±1V to ±10V. Isolation voltage, as with all isolated 3B's, is ±1,500 V (transformer-coupled), and inputs are protected from overvoltage up to 220 V rms.

- **AC signal conditioners** (3B42, 3B43, 3B44),* with full-scale ranges of 20 mV to 1 V (3B42), 1 V to 50 V (3B43), and 50 V to 550V (3B44), provide isolated rectification, filtering, and scaling.

Table I. Input Modules Selection

Input Type/Span	Voltage Output	Current Output	Nonisolated Modules	Isolated Modules
dc, ±10mV, ±50mV, ±100mV	±10V	4-20mA/0-20mA	3B10	3B30, 3B40
dc, ±1V, ±5V	±10V	4-20mA/0-20mA	3B10	3B31, 3B41
dc, ±10V	±10V	4-20mA/0-20mA	3B11	3B31, 3B41
dc, 4-20mA, 0-20mA	0-10V	4-20mA/0-20mA	3B12	3B32
Thermocouple Types J, K, T, E, R, S, B	0-10V	4-20mA/0-20mA		3B37
100Ω Platinum RTD, 2, 3, 4 wire α = 0.00385 (linearized)	0-10V	4-20mA/0-20mA	3B14	3B34
100Ω Platinum RTD, Kelvin 4-wire α = 0.00385 (linearized)	0-10V	4-20mA/0-20mA	3B15	
Strain Gage ±30mV, ±100mV	±10V	4-20mA/0-20mA	3B16, 3B18	
AD590/AC2626 Solid State Temperature Transducer	0-10V	4-20mA/0-20mA	3B13	
ac, 0–50mV rms, 0–100mV rms	0–10V	4-20mA/0-20mA		3B42
ac, 0–10V rms	0–10V	4-20mA/0-20mA		3B43
ac, 0–150V rms, 0–250V rms	0–10V	4-20mA/0-20mA		3B44
Frequency 0–25Hz, 0–300Hz	0–10V	4-20mA/0-20mA		3B45
Frequency 0–1500Hz, 0–3000Hz, 0–25kHz	0–10V	4-20mA/0-20mA		3B46

Their principal use is to monitor line voltage and ac current.

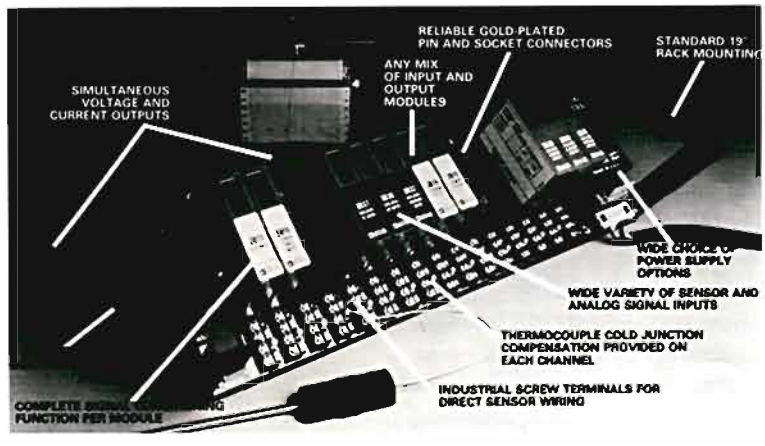
- **Frequency-input conditioners** (3B45, 3B46)* convert frequency to voltage, to within 0.1%, with full-scale ranges of 25 Hz to 1,100 Hz (3B45) and 520 Hz to 25 kHz (3B46). Frequency sources include switch closures, ac generators, photodetectors, and flowmeters.

STRAIN-GAGE CONDITIONERS

The 3B18 is a wideband input module designed to accept signals from full four-arm-bridge strain-gage transducers, connected to its screw terminals (Figure 1). It provides a switch-selectable excitation of +3.3 V or 10.0 V and can be used with bridges having impedance from 100 ohms to 10 kΩ; its 20-kHz bandwidth lets it serve in dynamic, as well as dc, strain-gage applications.

The excitation is applied via screw-terminals 1-4, and the bridge output is connected to terminals 2-3. Both input and excitation circuitry, which are typically connected to field wiring, are protected against differential voltages up to 130V ac. The 3B18 is available either with externally programmable gain, or optionally with fixed input scales of 30 mV (3 mV/V for 10 V) or 10 mV (3 mV/V for 3.3 V). The AC1310 ranging card—which plugs onto 3B modules—is employed with user-supplied resistors to set desired gain values—and capacitors to limit bandwidth.

Standard outputs are: voltage, ±10V at up to 2 mA, and (simultaneously) current, 0 to 20 mA or 4 to 20 mA, with load resistances



*Use the reply card for technical data.

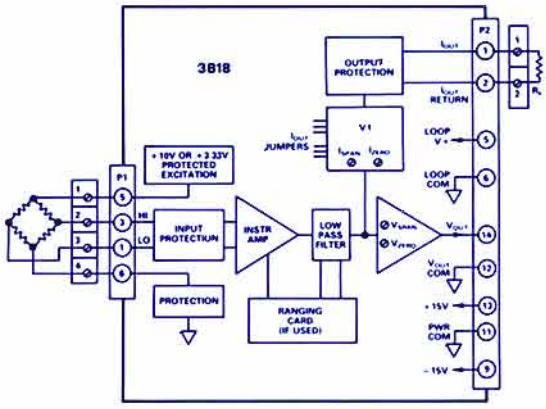


Figure 1. 3B18 strain-gage conditioner.

up to 850 ohms. All 3B Voltage outputs (which usually connect to a data-acquisition or control system) are protected against shorts to ground; current outputs (which may be connected to field wiring) are protected against 130 V rms.

WIDEBAND DC SIGNAL CONDITIONERS

Model 3B40, an isolated wideband millivolt-input module, accepts signals ranging from ±10 mV to ±100 mV full-scale; the 3B41 similarly accepts signals from ±1 volt to ±10 V full-scale. To handle signals with substantial frequency content, both modules have 10-kHz bandwidth, established by a 2-pole filter (expandable to 3 poles). Voltage and current outputs are standard, as described above.

Figure 2 shows the functional diagram of both devices. Transformer coupling provides stable galvanic isolation of up to ±1,500 V between input and output; the input terminals are protected against 220 V rms input; and the current output is protected

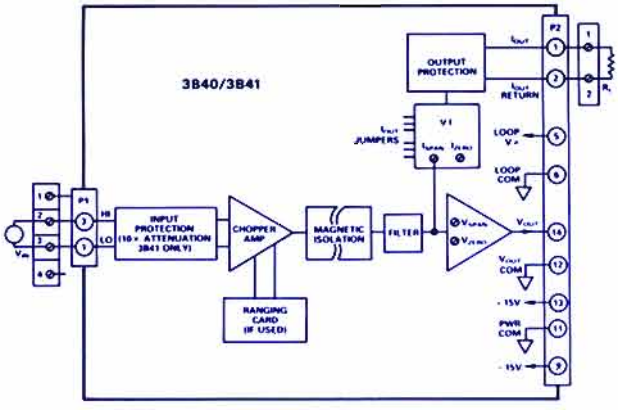


Figure 2. 3B40/3B41 wideband dc signal conditioners.

against 130 V rms. Voltage and current outputs (as is the case with all 3B modules) are adjustable over ±5% of span range for both zero and span, via potentiometers accessible from the front panel.

Both types are available with either externally programmable gains or a choice of 3 fixed input spans: ±10/50/100 mV (3B40) and ±1/5/10 V (3B41). The externally programmable units, employing the AC1310 and user-supplied resistors, may also be connected for zero-suppression voltage (up to ±3.175 V for 3B40 and ±31.75 V for 3B41).

AC SIGNAL CONDITIONERS

Models 3B42, 3B43, and 3B44 are designed to accept ac sine-wave signals, at line frequencies from 50 Hz to 400 Hz, and provide dc output voltage proportional to the average value, scaled rms. They are designed for monitoring power-line voltages and (using shunts) currents. The three models deal with three ranges of full-scale rms voltage: 20 mV to 1 V rms (3B42), 1 V to 50 V rms (3B43), and 50V to 550 V rms (3B44). As with the other modules, options exist for external programming, using the AC1310 ranging card, or choices of fixed ranges.

The input signal is average-rectified, filtered, scaled to give an rms reading for sine-wave input, and transformer-coupled to the output via an isolation stage. Inputs of the 3B42 and 3B43 are protected against voltages up to 220 V rms, and the 3B44 is protected against voltages up to 550 V rms. As with the other isolated modules, the common-mode isolation voltage is ±1,500 V. All isolated modules meet IEEE Standard 472 for transient protection (SWC). Both voltage and current outputs are available; the voltage range for these modules is 0 to +10 V. As with the others, the current output is protected against 130-volt ac faults.

FREQUENCY-INPUT CONDITIONERS

Model 3B45 is a transformer-isolated frequency-input module that is designed to accept signals with amplitudes from 10 millivolts to 220 volts rms, or switch closures, having full-scale frequencies ranging from 25 Hz to 1,100 Hz full-scale, and provide voltage and current outputs proportional to the frequency. Model 3B46, a similar device, has full-scale frequencies from 520 Hz to 25 kHz. Both modules have user-selectable thresholds of either 0 V, for normal ac signals, or 1.6 V, for digital logic signals, and an internal pullup resistor for use with switch-closure inputs.

Figure 3 shows a functional block diagram for both models. Input protection is provided at all four screw terminals. The input signal is compared to the selected threshold and hysteresis, and the comparator's output frequency is converted to voltage. The signal is then amplified and filtered to give the high-level voltage output.

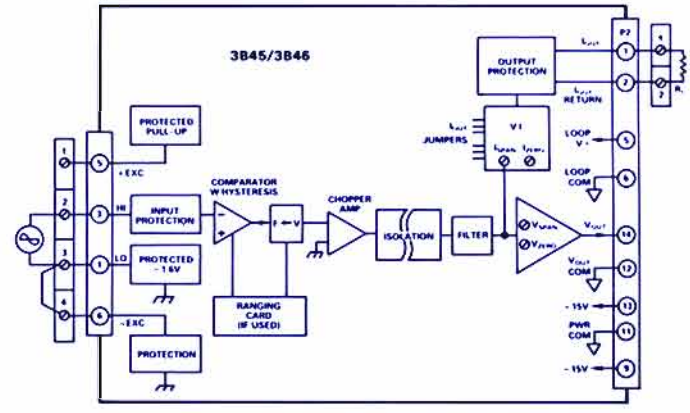


Figure 3. 3B45 and 3B46 frequency-input conditioners.

As with the other modules, the 3B45 and 3B46 are available with either externally programmable ranges or a choice of fixed ranges: 0-25 Hz or 0-300 Hz (3B45) and 0-1.5 kHz, 0-3 kHz, or 0-25 kHz (3B46). The externally programmable modules, when used with the AC1310 ranging card, also have the possibility of modifying the hysteresis range (normally jumper-selected as either 0 or ±20%), using external resistance.

CONCLUSION

These products join the 3B Series, which includes output modules, as well as input modules that condition thermocouple, RTD, voltage (and mV), current, and AD590 IC temperature-sensor inputs. With even more on the way, the 3B Series is fast becoming the most-versatile available solution to signal-conditioning problems.

8-BIT CMOS DAC

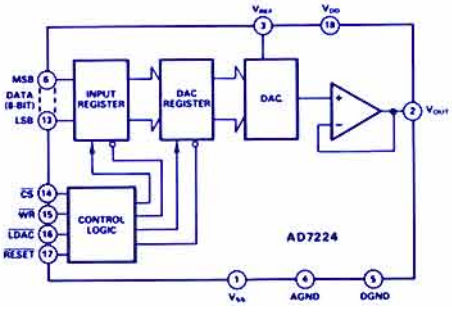
Voltage Output
Double-Buffered Input

The AD7224* is a monolithic 8-bit CMOS microprocessor-compatible d/a converter (DAC) in an 18-pin dual in-line package. Designed for a variable or fixed external reference, it is a complete voltage-output device, with double-buffered data inputs and an on-chip output amplifier. Because of its low total unadjusted error—less than 1 LSB over temperature (L, C, and U grades)—it requires no adjustments.

Its high-speed logic allows direct interfacing to most microprocessors. The double-buffered interface logic consists of an input register and a separately enabled DAC register. This arrangement allows the input register to be updated at the convenience of the µP, while the DAC is updated whenever necessary. As a result, a number of DACs can be primed separately by the microprocessor, without changing their existing output levels, then enabled to deliver their new outputs simultaneously, a useful feature in (e.g.) test equipment.

A low-dissipation device (typically 35 mW with a single supply), the AD7224 will operate with either a single positive supply, and a +10-volt reference, or dual supplies and a +2 to +12.5-volt reference. The output amplifier can develop 10 volts across a load of 2 kΩ.

The device is fabricated using the Analog Devices Linear-Compatible CMOS (LC^{2}MOS) process, specifically developed to permit both high-speed digital logic and precision analog circuits to be integrated on the same chip. The AD7224 is available in six grades, three temperature ranges, and 3 packages, with prices starting at $4.95 (100s, commercial grade, plastic).



*Use the reply card for technical data.

4-CHANNEL 12-BIT CMOS A/D CONVERTER

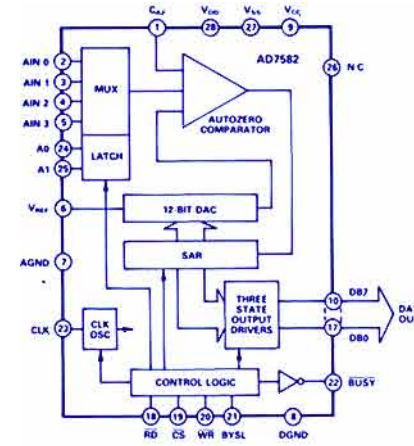
µP-Compatible Low-Power AD7582 Converts in 100 µs
Total Error < ±1 LSB, No Missing Codes over Temperature

The AD7582* is a monolithic 4-channel 12-bit CMOS a/d converter (ADC) in a 28-pin dual in-line package. All versions have total unadjusted error less than ±1 LSB max (including no missing codes and offset error less than ¼-LSB max) over the operating temperature range.

The AD7582 is designed for easy interfacing to 8-bit microprocessors, using standard control signals: $\overline{CS}$ (decoded device address), $\overline{RD}$ (read), and $\overline{WR}$ (write). Right-justified conversion results are available in two bytes (8 LSB's and 4 MSB's), readable in either order. Two BUSY flags are available for versatile interfacing—one as a control signal, the other as the MSB of the more significant data byte.

A successive-approximation device, the AD7582 has a per-channel conversion time of less than 100 µs. An autozero phase occurs at the start of each conversion cycle, resulting in low system offset voltages, typically less than 100 µV. Low dissipation, typically 75 mW, is inherent.

Three versions are available, for three temperature ranges. Prices start at $32.50 (AD7582KN—commercial temperature range, plastic, 100s).



TWO 12-BIT DACS IN 0.3" 20-PIN PACKAGE

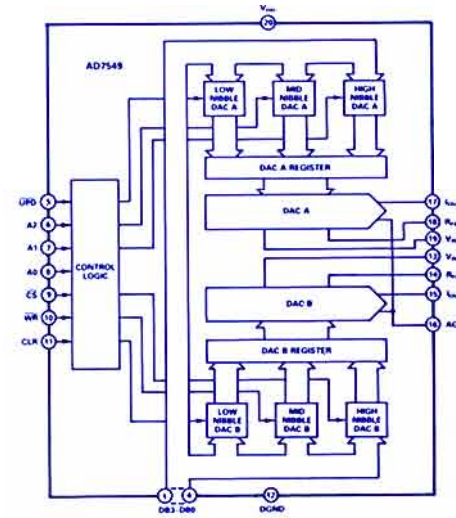
4-Quadrant Multiplying DACs Interface in 4-Bit Nybbles
AD7549's Independent DACs Share Bus, Are Double Buffered

The AD7549* contains a pair of 12-bit CMOS 4-quadrant multiplying digital-to-analog converters fabricated on a single monolithic silicon chip. This compact structure allows the device to be packaged in a low-cost, space-saving 0.3" 20-pin DIP.

Sharing a common internal 4-bit bus, both converters are double-buffered; thus, the AD7549 is compatible in speed and easily interfaced with most microprocessors. It accepts TTL, 74HC, or 5-V CMOS logic inputs. It is available in a choice of grades, temperature ranges, and packages, and priced from $16.95 (AD7549JN in 100s).

Since both DACs are fabricated on the same chip, excellent thermal tracking and gain error tracking between the two DACs is ensured, opening up applications in programmable filters, stereo systems, and X-Y resolvers, plotters and displays.

The input registers for each DAC are loaded separately in 3 nybbles; their contents may then be latched into the respective DACs—or both DACs may be updated simultaneously—upon command. The latches are structured for easy sequential loading.



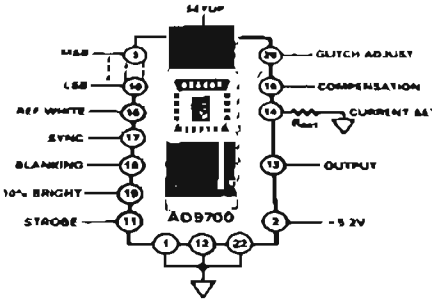
MONOLITHIC 8-BIT RASTER-DISPLAY DAC

AD9700 Updates Displays at Rates up to 125 MHz
Replaces Equivalent Dedicated-DAC Hybrids and Modules

Three years ago, in these pages (*Analog Dialogue* 15-2), the HDG-0805,* the first 8-bit hybrid display DAC, was introduced. Now, the monolithic AD9700,* industry's first monolithic DAC to combine an on-chip reference with composite controls for raster-scan graphics at update rates as high as 125 MHz, has become available for applications in high-speed display applications—including color graphics, test equipment, and TV video reconstruction.

The DAC's 8-bit resolution provides 256 (2^8) levels of gray-scale (standard white to black) intensity, with settling time of 10 nanoseconds to 0.4%. Full-scale integral and differential nonlinearity are typically ±0.2%, and the 17-mA full-scale output current permits the DAC to drive 75-ohm loads directly. Price is $32 in 100s.

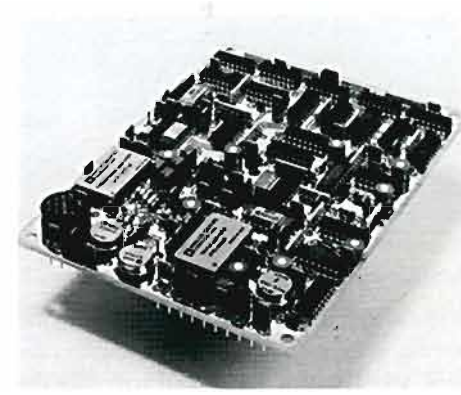
On-chip blanking, composite sync, and



10% brightness and reference-white control provide compatibility with EIA standards RS-170 and RS-343. The on-chip data latches reduce external support circuitry and help to achieve the low output-glitch impulse specification of 50-picovolt-seconds (further reducible by external trimming) to prevent display perturbations. Logic compatibility is ECL, but adaptable to TTL where slower update rates are involved.

10-BIT 20-MHz ADC

With On-Board Track-Hold
Complete on a Single Card



Model CAV-1020* is a complete 10-bit a/d conversion subsystem, with a guaranteed maximum conversion rate of 20 MHz (typically 25 MHz). Complete on a 5" × 7" circuit card, it includes a track-hold, a two-step flash converter with digitally corrected subranging, and all necessary timing circuitry, components, and calibration adjustments. It requires only power supplies and an encode command.

While it is pin-compatible with the earlier MOD-1020, and its applications are similar, its highest-speed options are both faster and lower in cost than the corresponding options of MOD-1020 ($2,997 in small quantity).

Its applications include high-speed digitizing in transient analyzers, medical electronics, radar systems, digital oscilloscopes, and general high-speed instrumentation. All digital inputs and outputs are ECL-compatible; analog input impedance is 1000 ohms.

DC accuracy is to within 0.05% ± ½ LSB. Dynamically, its in-band harmonics are 50 dB below full-scale for frequencies between 5 MHz and 10 MHz (maximum allowable input frequency at 20-MHz sampling), dropping to -60 dB at frequencies from dc to 1 MHz.

Its signal-to-noise ratio, with 500-kHz analog input, is 63 dB; noise-power ratio is 45 dB, for dc to 8.2 MHz white noise, with a slot frequency of 3.886 MHz and encode rate of 20 MHz. Two-tone linearity error for 4.996 and 4.998 MHz is 52 dB (min) below full scale; and differential gain and phase in units optimized for video applications are 1% and 0.5°, for 20 IRE-unit reference.

3 COMPLETE NEW SAMPLING A/D CONVERTERS

Combine High Resolution and Low Power Consumption
On-Board Sample/Hold, Reference, 3-State Output Buffers

The DAS1157, DAS1158, and DAS1159* are the lowest-powered single-channel 14-, 15-, and 16-bit data-acquisition systems available in the industry. They are *complete*: the compact (2" × 4" × 0.375") metal package contains a high-resolution a/d converter with a + 10-volt reference, sample-hold amplifier, 3-state output buffers for interfacing to an 8- or 16-bit bus, trim potentiometers for gain and offset, and power-supply bypass capacitors.

The DAS1157 and DAS1158, with their lower power consumption, higher max throughput rate, and all-hermetic semiconductors, will serve as plug-compatible improved replacements for the A/D/A/M-834 and 835, while the DAS1159 stands alone as the only 16-bit—resolution sampling ADC currently available.

The DAS Series' low power consumption, rugged package, and temperature range of

−25°C to +85°C for rated performance suggest applications such as seismic data acquisition and portable instrumentation.

Key max specs for the DAS1157/58/59 include: differential nonlinearity, ±0.003/0.0015/0.0015%; integral nonlinearity, ±0.005%/0.003%/0.003%; differential nonlinearity tempco, ±2/1/1 ppm/°C; and gain tempco, ±8/8/8 ppm/°C. Max overall conversion time is 55 µs (18 kHz throughput rate), and aperture delay and jitter are 250 ns and 1 ns. Prices are $219/$263/$289 in 100s.

*Use the reply card for technical data.

RESOLVER/SYNCHRO-TO-DIGITAL CONVERTERS

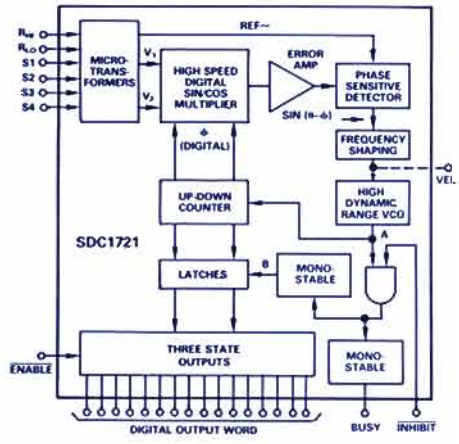
Two New 12- and 14-Bit Hybrids and a 16-Bit Module: Continuous Tracking, Internal Transformers, 3-State Latches

The SDC/RDC1767 and 1768* are hybrid 12- and 14-bit converters in 0.28"-high hermetically sealed 32-pin metal DIPs. They combine high tracking rates (36 rps, 12 bits; 16 rps, 14 bits) with velocity output (see pp. 16-17) and transformer isolation (350 V dc). Tracking is continuous, and data can be transferred to the bus via the 3-state output buffers without opening the tracking loop.

Typical applications include antenna monitoring, artillery fire control, jet-engine control, and avionics. Signal and reference frequency range is from 400 Hz to 2.6 kHz; a dc error output is available for use as a Built-In Test Equipment (BITE) checkpoint.

Maximum error is guaranteed at ±8.5 and ±5.3 arc-minutes (1767 and 1768), over the full −55°C to +125°C case-temperature range. Prices are $471 and $504 (10-24).

The SDC/RDC1711* is a 16-bit converter, housed in a low-profile (0.4" high) module, designed for high-accuracy (±1.3 arc-minutes over the entire temperature range) angle-measurement applications. It has an 8-rps tracking rate and fast step response. Price is $574 in small quantity.



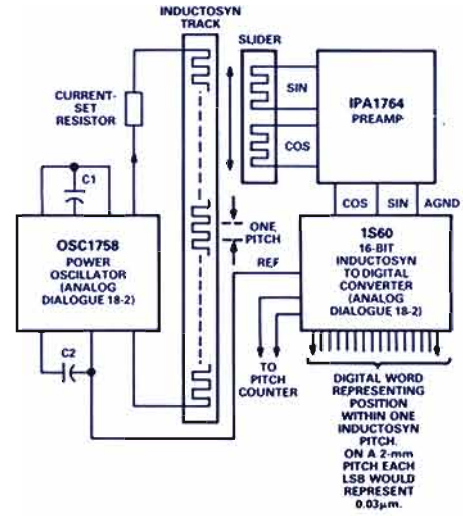
HYBRID INDUCTOSYN PREAMPLIFIER

IPA1764 Amplifies Signals from the Inductosyn Slider Provides Correct Levels to Inductosyn/Digital Converter

The IPA1764* is a matched pair of high-gain preamplifiers in a hybrid package, designed to amplify low-level output signals from the Inductosyn† slider and scale them correctly for Inductosyn-to-digital converter inputs. It is available for both commercial and military temperature ranges. Prices are $98/$106 (100s).

The functional diagram shows how the IPA1764 is used with an Inductosyn and the 1S60 16-bit Inductosyn-to-digital converter. The OSC1758 power oscillator (introduced with the 1S60 in *Analog Dialogue* 18-2) provides excitation to the Inductosyn and a reference signal to the converter. The three hybrid devices, used with a dc power supply, provide all the electronics necessary for interfacing the Inductosyn to a digital controller.

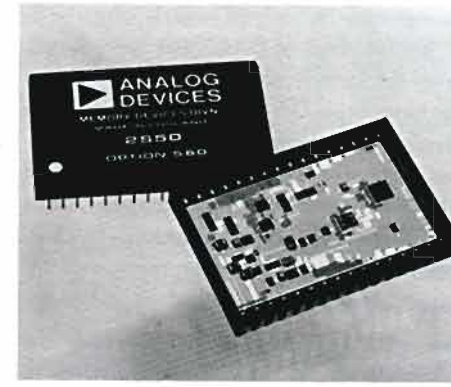
Inductosyn systems provide very-high-resolution linear and rotary measurements in numerical control, flat-bed and drafting machines, tracking radars, satellite antennas, and gunsights.



*Use the reply card for technical data.
†Inductosyn is a registered trade mark of Farrand Controls, Inc.

LVDT/DIGITAL

2S50 11-Bit Hybrid Converter First in the Industry



The 2S50* converts ac signals to an 11-bit parallel digital word. When used with an LVDT or RVDT (Linear/Rotary Variable Differential Transformer), the digital output represents the linear or rotary displacement of the transducer. In addition, the 2S50 can also be used as a general-purpose ac ratiometric a/d converter—compatible with load cells, strain-gage bridges, and some pressure transducers and interferometers.

LVDTs are widely used wherever displacements of a few micro-inches to several feet can be measured directly, or where other quantities, such as force and pressure can be converted to linear displacement. Typical applications of LVDT measurement systems are in industrial measurements and gauging, numerical control, avionic control systems, valves and actuators, and limit sensing.

2S50 series converters, assembled in a 32-pin hybrid package, translate the outputs from LVDT and RVDT transducers into digits *directly*. No signal conditioning, trims, preamplifiers, demodulators, or filters are required. It is a tracking converter, operating on the *ratio* of two inputs; as a result, the whole system, consisting of excitation oscillator, LVDT, and 2S50 converter, is insensitive to changes in excitation voltage, amplitude, frequency, and waveshape.

The 2S50 is optionally available for either of two reference frequency ranges, 400 Hz (fixed), or 1kHz to 10 kHz, and for either the commercial or military operating temperature range. Prices start at $107 in small quantity.

FASTER TESTER

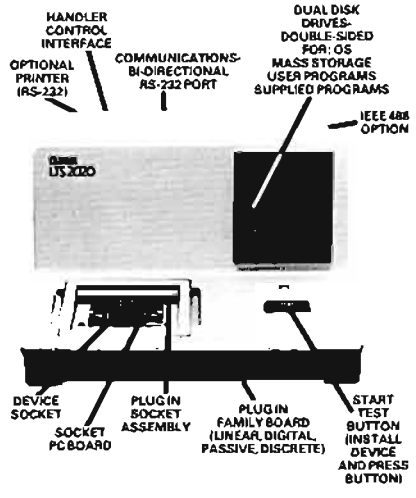
LTS-2020 is Fast, Versatile Has Increased Capabilities

The LTS-2020* is a new benchtop component test system that can perform high-speed ac tests on digital ICs—using an optional remote AC test head—in addition to maintaining and extending the LTS-2000 series testers' repertoire of test capabilities for linear, data-conversion, and discrete devices—with increased throughput and 16-bit accuracy.

The LTS-2020 executes instructions twice as fast as earlier LTS series testers; test times are reduced by as much as 50%. Configured for ac digital testing, the LTS-2020's tests include propagation delays, setup and hold times, pulse width, and rise and fall times for CMOS and TTL devices. Optimizing the cost-performance tradeoff, it is the only tester currently available to offer ±1.5-ns accuracy and 500-ps resolution at benchtop prices; less than $50,000.

It is well-suited for both incoming inspection and production testing, fully compatible with automatic handlers and probers, and comparable to mainframe testers in test times.

Programmable in BASIC, it will run programs developed on other LTS test consoles. This allows users of existing programs to upgrade speed and memory-address capacity for testing op amps, converters, timers, comparators, regulators, switches, diodes, transistors, and FETs. 84K of its 128K memory is user-available. It is compatible with all 2000-series test hardware.



*For technical data, use the reply card.

MEASUREMENT & CONTROL: 2 NEW MACSYMS

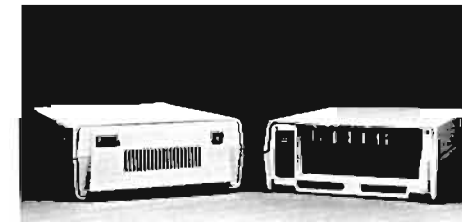
MACSYM 250: Interface Cards, Number Crunching, & 512K RAM

MACSYM 260: Ruggedized Stand-Alone Controller

The MACSYM™ 250* programmable Measurement and Control Unit can accept as many as 256 differential analog inputs or deliver 64 analog outputs. In addition to its data-acquisition functions, similar to those of the MACSYM 200 (*Analog Dialogue* 16-3), its powerful microprocessor/math coprocessor architecture gives fast program execution. It has multitasking MACBASIC™ for real-time performance, and up to 512K of RAM.

Besides data acquisition, it can perform such functions as local limit checking, data analysis, and generation of statistical reports and control outputs. This reduces system communications, increases throughput, and accelerates response to real-time events.

Compatible with IBM PCs, with a kit, it communicates at high speed with a workstation—a MACSYM 150 or special IBM-built MACSYM 121—at 307 kB, via one of its ports. The other can communicate with a local terminal or printer (RS-232) at 19 kB.



The MACSYM 260*, a hardened stand-alone measurement-and-control unit with the same computing, I/O, and RAM capabilities as the MACSYM 250, is industrially packaged, with rugged metal construction, for rack, NEMA, or wall mounting, with all connections available from the front. With 384K of PROM, programs are retained in non-volatile memory for stand-alone operation. It can also communicate with other computers via RS-232 or 20-mA current loops.

™MACSYM and MACBASIC are trade marks of Analog Devices, Inc.

TWO NEW CARDS FOR MACSYM 200 and 150

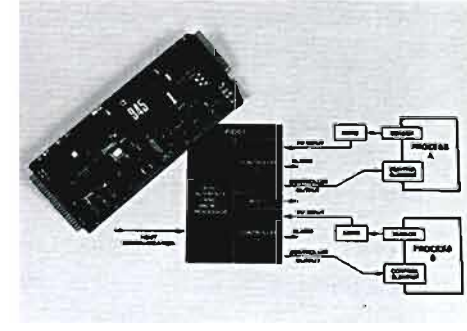
PID01—Dual-Loop Controller Card: MACSYM 200, 250, & 260

DSI101—Series 100 Serial Interface Card for MACSYM 150

Each of the two channels of the PID01* provides P-I-D control for pressure, flow, temperature, and other process and batch parameters. A high-level process-variable input signal from the loop is compared with the setpoint value. Deviation, or error, is calculated, and then integral and differential terms are developed and combined according to the PID algorithm. A control output is generated as a 0-to-20 mA or 4-to-20 mA signal and sent to the final control element or actuator. Typical applications occur throughout the process industries.

The PID01's on-board microprocessor updates each loop every ½-second, regardless of other computational loads on MACSYM. The tuning parameters (coefficients) can be changed during the process to implement adaptive control functions.

The DSI101* card makes available two independent asynchronous channels for serial



interfacing in MACSYM 150 and 350 systems. One channel provides an RS232/423 or RS422 interface, the other provides RS232/423 or a 20-mA current-loop (active or passive) interface. The DSI101 has a jumper-selected choice of compliance voltage for the current loop—5 V or 30 V.

The card connects a MACSYM 150 or 350 to peripherals or another computer. Users can set 16 baud rates, from 50 B to 19.2 kB.

Worth Reading

FREE NEW PUBLICATIONS FROM ADI*

Application Note

"CMOS D/A Converter Circuits for Single +5-Volt Power Supplies," by Phil Burton. How to use CMOS d/a converters in μP-based systems when only a single +5-V supply is available. Topics include: voltage-switching operation, single-supply current-steering operation, choosing the amplifier, interfacing single +5-volt DACs to processors, and the design of an X-Y plotter interface.

Reprints of articles from the trade press

"Getting the Most from High-Resolution D/A Converters," by Scott Wayne, *Electronic Products*, December 12, 1983—a close look at DAC specs, requirements, error sources, and test methods—and how they can affect your circuit designs. Topics include: nonlinearity, programmed measurements, summation errors, instrumentation, factory applications, waveform-reconstruction specs, eliminating glitches, and checking total harmonic distortion.

"Linear V-f Converter Chip Invades Module Territory," by Lawrence M. DeVito, *Electronic Design*, February 23, 1984. A 1-MHz V-f converter (the AD650) permits the construction of systems needing high-resolution a-d converters, variable-frequency clocks, and phase-locked loops having a wide tracking range.

MCDigest

MCDigest, "The Measurement and Control Digest published by Analog Devices, Inc.," is a quarterly publication of applications information, user feedback, and general information on system products of ADI's Measurement and Control Division. Featured in Volume 4, Number 1 (July, 1984): displaying task states in a MACSYM 150 system, interfacing the 3B series to MACSYM, interfacing Televideo 925 terminals to MACSYM, command file techniques, software for the MACSYM—DAIS and MACANALYSER. Also included are 6 new-product briefs and a like number of "customer-service" items.

New Brochures

"DAIS—Data Acquisition Information System" is an easy-to-use, MACSYM-based menu-driven program for flexible data acquisition, data interpretation, and control. This 6-page brochure describes DAIS, where it is used, and benefits to automation projects.

"It Never Blinks" THE EYE™ from Analog. Vision for the factory of the future is a colorful 8-page brochure, including a pocket filled with data sheets on the IVS-100 (featured in this issue).

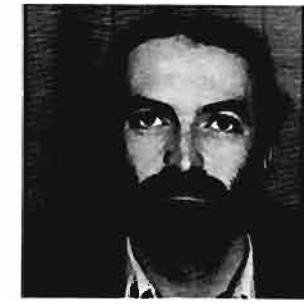
"Converter Products for Your Sensor Interface" is an appetizing 12-page brochure describing the products and technologies of our Memory Devices Division in the field of transducer data conversion. Ask for the Memory Devices brochure.

MORE AUTHORS *(continued from page 2)*

Reg Gillmor (page 6) recently joined ADI's Machine Vision Marketing staff, with responsibilities in product documentation and training. Reg attended the University of Michigan for his undergraduate education, and did graduate work at the University of Maine, receiving a Ph.D; he also spent two years as a Special Research Student at Hiroshima University (Japan). Before coming to Analog Devices, he worked for four years at EG&G.

Patrick Helsingius (page 8) is an Applications Engineer in the Machine Vision Products group at ADI. A native of Finland, he came to the United States following his graduation from the International School of Brussels. Patrick joined Analog Devices after earning a BSEE from Brown University.

Kimberly Mager (page 10) is on the Machine-Vision Applications staff at ADI. She attended Brandeis University and was graduated in 1980 with a BA in Chemistry. Before joining ADI, she worked for four years at Rigaku/USA, Inc., a manufacturer of analytical X-ray instrumentation, as a Marketing Specialist.



Paul Nickson (page 16) is a Project Engineer on Resolver-to-Digital Converters at the Memory Devices division of Analog Devices, in East Molesey (Surrey), England. He was graduated from Birmingham University with a B.Sc. (with honours). Before joining ADI, he worked as an IC designer for Ferranti, Ltd., in Manchester, on voltage references, d/a and a/d converters, and telecommunications related products. His interests include woodworking and air-rifle shooting.

Sandra Perry (page 10) is a Marketing Specialist in ADI's Machine-Vision Products group. She received her undergraduate degree in Chemistry from Wellesley College. After working as a Scientist in the Research Division at Polaroid Corporation, she entered into graduate studies at MIT's Sloan School of Management. At Analog Devices, before joining the MVP group, she was a member of the Strategic Planning department.

Steve Zoeller (page 8) is an Applications Engineer in the Analog Devices MVP group. He joined ADI in June of this year, after graduating from the University of Rochester with a BS in Optical Engineering and Computer Science. While an undergraduate, Steve worked in the Laboratory for Laser Energetics and wrote software for image processing, computer graphics, and laser diagnostics.

*Use the reply card to request a copy.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE . . . (Volume 18, Number 2, 1984 — 28 pages):

Single-Port Multiplier-Accumulator Saves Hardware and Real Estate (ADSP-1110)
The Compleat General-Purpose 12-Bit D/A Converter (AD667)
Speed Up FIR Filters
Flash Converters Work Better with Track/Holds
First 12-Bit, 1-MHz Hybrid A/D Converter with Track/Hold (HAS-1201)
Generate Precision Square and Triangular Waves with AD630 Balanced Modulator/Demodulator
Flexible Monolithic Instrumentation Amplifier (AD625)
Thermocouple-Based Setpoint Controllers (AD596 & AD597)
Autoranging Microprocessor-Based RTD/Thermistor Meters (AD2060/61)
New Hybrid Resolver-to-Digital Converter Family (1S20/40/60/61)
Low-Cost 12-Bit Analog Interface Boards for VMEbus (RTI-600)
New-Product Briefs:
- 16-Bit Hybrid A/D Converter (AD ADC71/72)
- 8 X 8 Monolithic CMOS Multiplier with Unsigned Format (ADSP-1081)
- Low-Cost Precision FET Op Amp (AD611)
- Double-Buffered 14-Bit CMOS Multiplying DAC (AD7534)
- Analog Devices "The Eye™" Intelligent Vision System (IVS-100)
- Power Oscillator for Resolvers (OSC1758)

Worth Reading: New publications from Analog Devices, ADI in Trade Press
Editor's Notes, Authors, Potpourri, Advertisement (AD7226 Quad 8-Bit DAC)
Erratum . . . Editor's Note on page 2, second paragraph, second sentence. Correct numbers are given in: "Plotted on a log-log scale, this function approximates a straight line with a slope of about -0.3 to -0.5."

NEW PUBLICATIONS AND SOFTWARE . . . The red-covered 1,920-page two-volume Analog Devices 1984 Databook is now available. Volume I: Integrated Circuits; Volume II: Modules & Subsystems. If you have not yet received your free copy – and want one – use the reply card, or call Analog Devices . . . A 2-page flyer with 2 family photographs and 10 functional diagrams succinctly describes our lines of isolation amplifiers and modular signal conditioners. Ask for Signal Conditioner/Iso-Amp flyer . . . The MACSYM PASCAL package is now available; it is a powerful software development package that allows the user to develop real-time measurement-and-control software using the PASCAL MT+86 compiler with MACSYM process I/O, graphics, and IEEE commands. Consult ADI Systems Sales.

DATA-SHEET ERRATA . . . 1984 Databook, Volume II, page 20-2 (power supplies): For 4.5 W, 6 W, 12 W models, Max line and load regulation are 0.07%; Load regulation for 1 W and 1.8 W models is 0.4% . . . AD9000 Data Sheet, page 5, and page 10-171 in 1984 Databook, Vol. I: In the 4th paragraph ("Like all flash converters, ..."), last sentence – input current increases and input resistance decreases in a series of small steps, etc. . . . DAS1128 module data sheet, connector should be AC1545 (corrected in 1984 Databook, Vol. II, page 15-12). Long dimension between mounting holes on P. C. board layout diagram should be 4.2 (106.68) – both data sheet and Databoook . . . ADSP-1009 and ADSP-1012 data sheets, and package G68A (1984 Databook, Vol. 1, page 19-20) – pin numbers on pin-grid package are as viewed from above.

PRODUCT NOTES . . . The AD2004 4 1/2-digit DPM converts at 4 per second; when externally triggered for higher conversion rates (to 8/s), accuracy will be decreased . . . The output of the 2B22 isolated voltage-to-current (4-to-20 mA) converter should be protected against voltage spikes when connected to cables exceeding 1 meter in length. This can be done simply by connecting a clamp diode (e.g., 1N4001) and a capacitor (0.1 uF, 60 V ceramic) in parallel across the 2B22 output. The diode's anode is connected to pin 14, cathode to pin 12 . . . Model 289J and 289K isolators have a pinout that is correctly described by the data sheet, the Databook, and markings on nearly all units. However, due to a unique occurrence, a small run of units (date codes 8417 thru 8426) are incorrectly marked. If you have units in this series, and would like them replaced at no charge, call Analog Devices Customer Service . . . Models ADC12QM and ADC1111 have a new conversion-time specification: 32 us max. Any unit with an "S" suffix on the date code has this specification . . . All new AD DAC71/72's will soon be packaged in a metal case. For information, consult your nearest ADI component sales office . . . The AD5240BD is the highest grade in its series, with 12-bit no-missing-code and drift specifications valid over -25°C to +85°C. For applications requiring -55°C to +125°C performance, we suggest the 10-us AD ADC85S-12 to replace the AD5240SD, which is not available . . . Recalibration service is available for high-accuracy d/a converters, such as DAC1136 and DAC1138. For details, consult ADI component sales.

PATENT . . . 4,460,891 to Norman B. Bernstein for "Analog-to-Digital Converter with Explicit Interpolation."

POWER SUPPLIES . . . The new, free 10-page 1984 Power-Supply Catalog, now available upon request, includes the latest specifications for all models of ac/dc supplies and dc/dc converters. It also includes a new two-year warranty for newly purchased supplies, which replaces the earlier 1-year warranty . . . 17 of the Analog Devices AC/DC power supplies have been listed by Underwriters' Laboratories (QQFU2: "Power Supplies for use in Data-Processing Equipment, Electronic and Office Appliances, and Business Equipment.") . . . Analog Devices DC-DC Converter prices have been substantially reduced. Check with your local sales office.

It's the new AD650 from Analog Devices—the first and only monolithic IC V/F converter to deliver 0.1% max nonlinearity at 1 MHz full scale frequency. But that's just the beginning. The AD650's performance advantage extends to lower full scale frequencies, too. At 10 KHz, for example, it provides 14-bit linearity. And it stays linear to 12 bits even when you get to 100 KHz.

Which means that for A/D conversion, the AD650 lets you optimize linearity, resolution or conversion rate to meet your exact system requirements. What's more, the inherently monotonic transfer function of a V/F gives you an A/D with no missing codes.

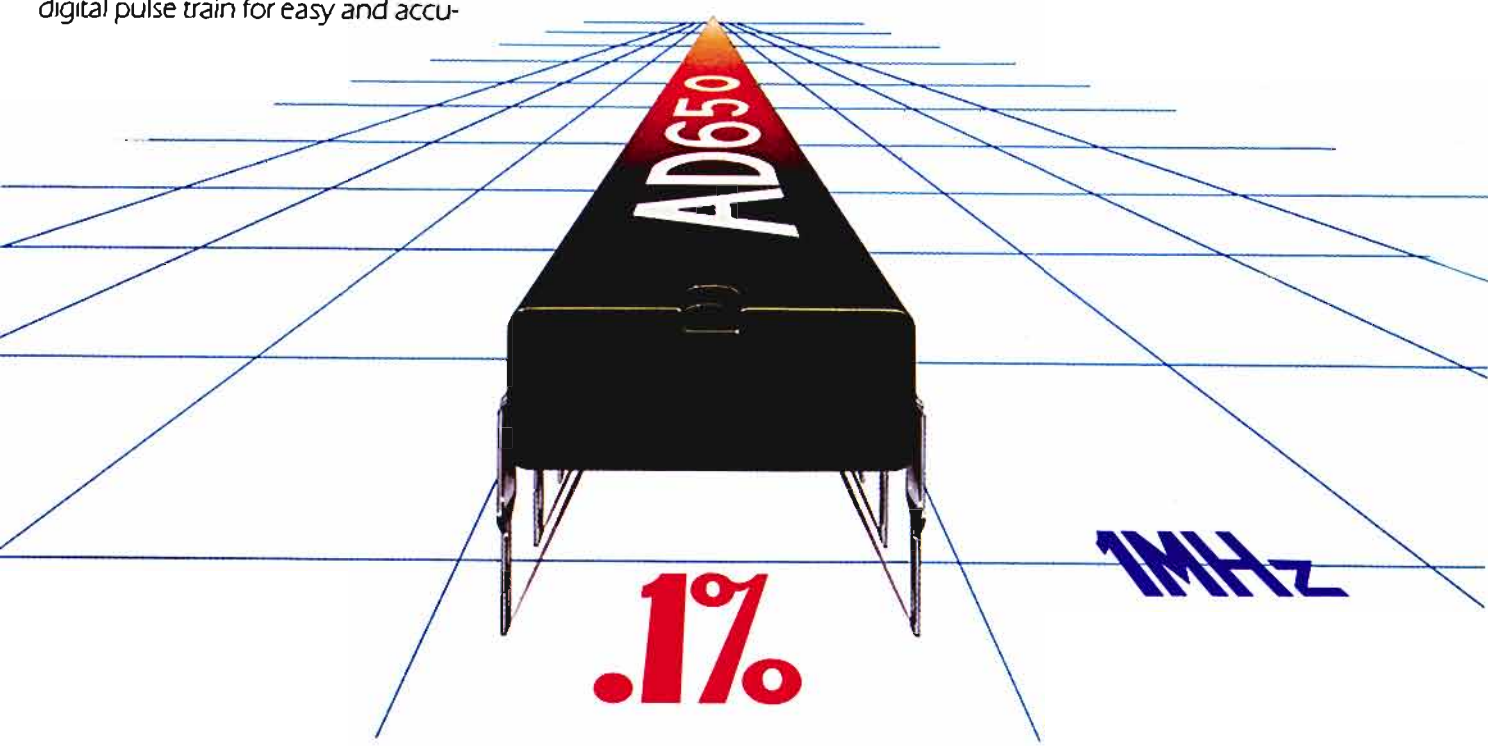
And of course, a superlinear V/F can convert an analog signal to a digital pulse train for easy and accurate transmission across an isolation barrier. The AD650 can serve as both a transmitter in V/F mode and as a direct or phase-locked loop type F/V-based receiver.

The AD650's versatile architecture accepts unipolar or bipolar input in the form of either current or voltage. And only the AD650 provides separate analog and digital grounds so you can keep 1 MHz output pulses and other digital noise out of the analog signal path.

Best of all, the AD650 is very competitively priced—it starts at just $7.15 in thousands.

For all the facts on the V/F performance leader, just call Applications Engineering at (617) 935-5565 or write Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062.

ANALOG DEVICES



At 1 MHz Only One V/F Converter Guarantees This Linearity.

Analog Devices, Inc., Two Technology Way, Norwood, MA 02062; Headquarters: (617) 329-4700; California: (714) 641-9391, (619) 268-4621, (408) 947-0633; Illinois: (312) 653-5000; New York: (716) 425-4101, (315) 437-5277; Ohio: (614) 764-8795; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094, (713) 664-6704; Washington: (206) 251-9550; Belgium: (3) 237 4803; Denmark: (2) 845800; France: (1) 687-34-11; Holland: (1670) 51080; Israel: (052) 28995; Italy: (2) 6883831, (2) 6883832, (2) 6883833; Japan: (3) 263-6826; Sweden: (8) 282740; Switzerland: (22) 31 57 60; United Kingdom: (01) 9410466; West Germany: (89) 570050

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